

CHELSEA DJ2 UMA Schematics Document

AMD Danube CPU S1G4

RS880M + SB820M

2010-05-15

REV : A00

DY : Nopop Component
HDMI : Pop for HDMI function
GIGA : Pop for GIGA LAN
10/100 : Pop for 10/100 LAN

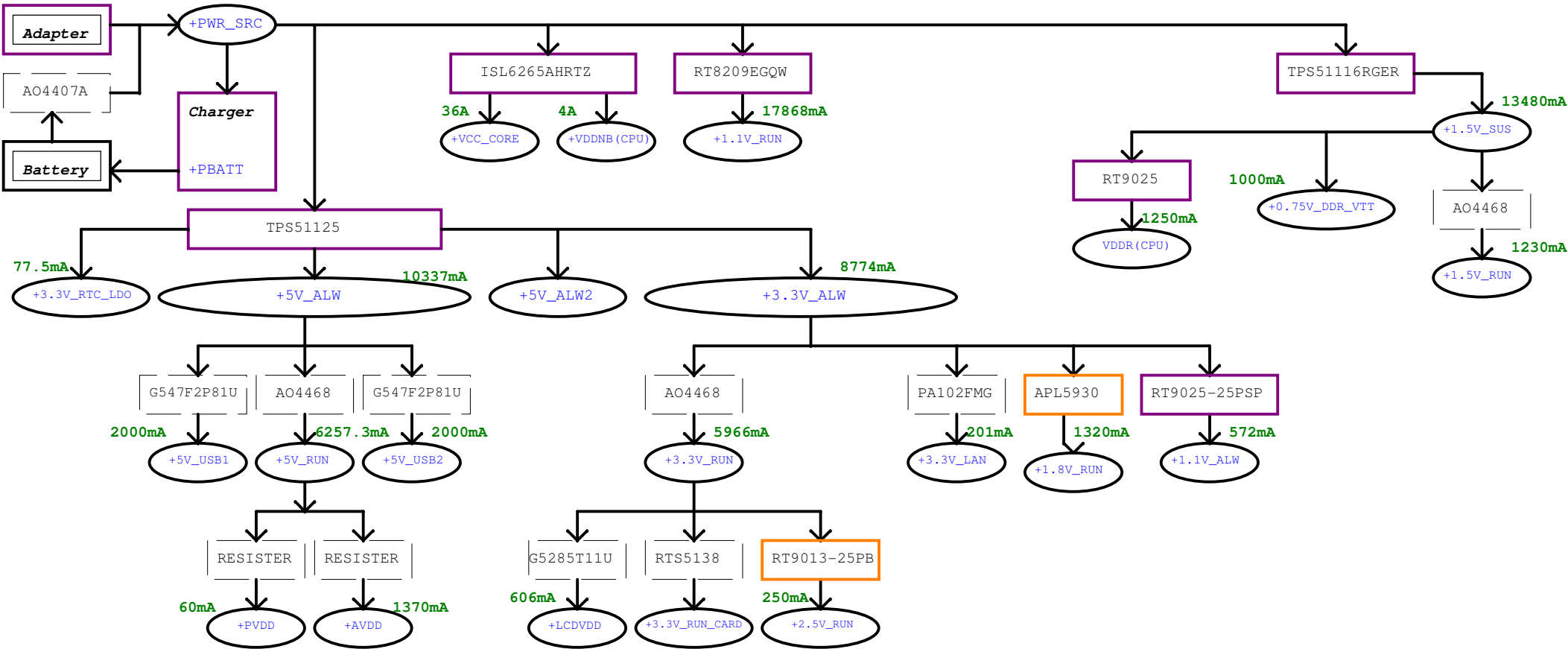
Power Block Diagram

Power Shape

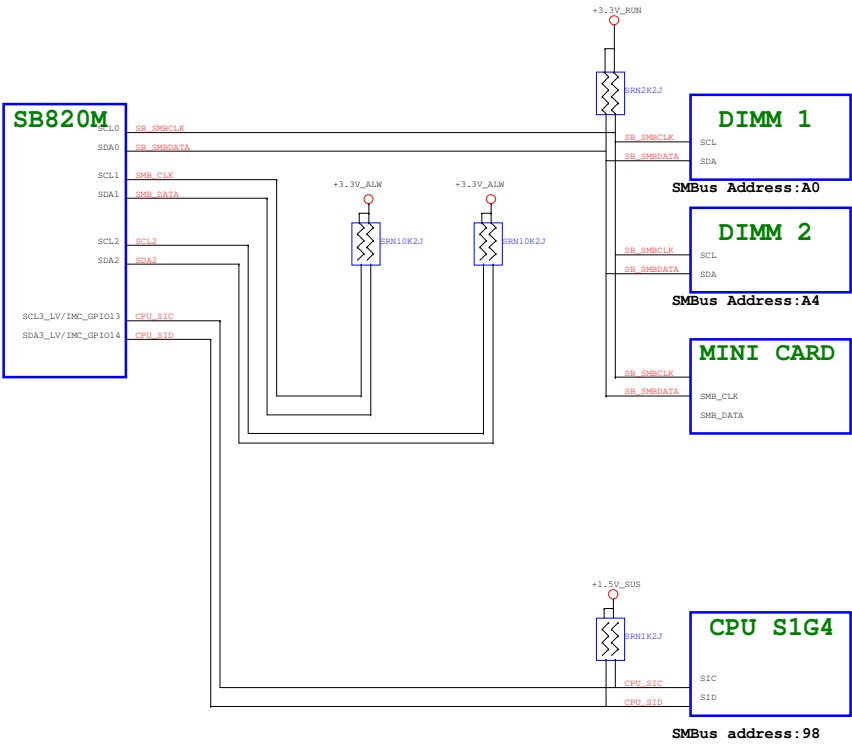
Regulator

LDO

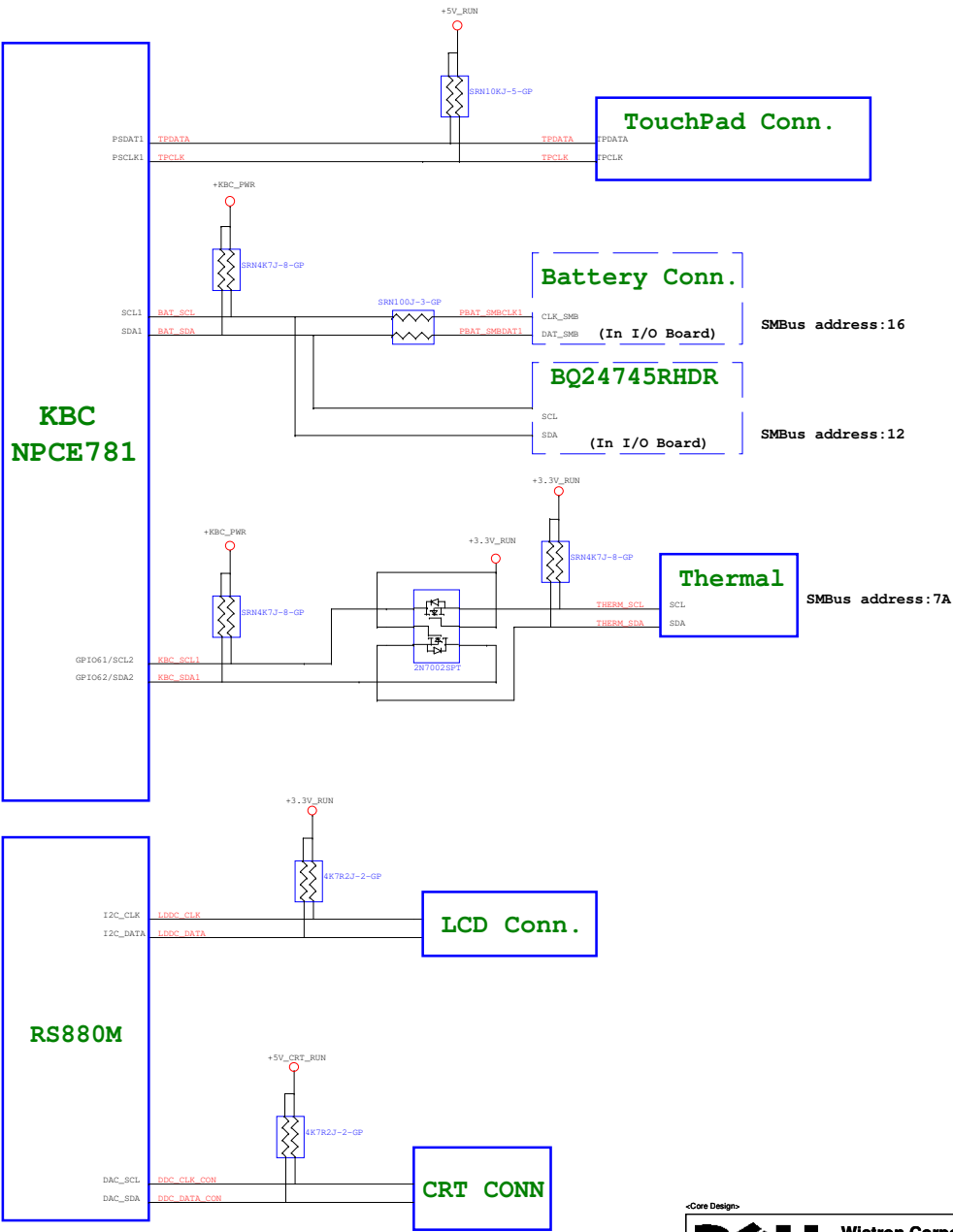
Switch



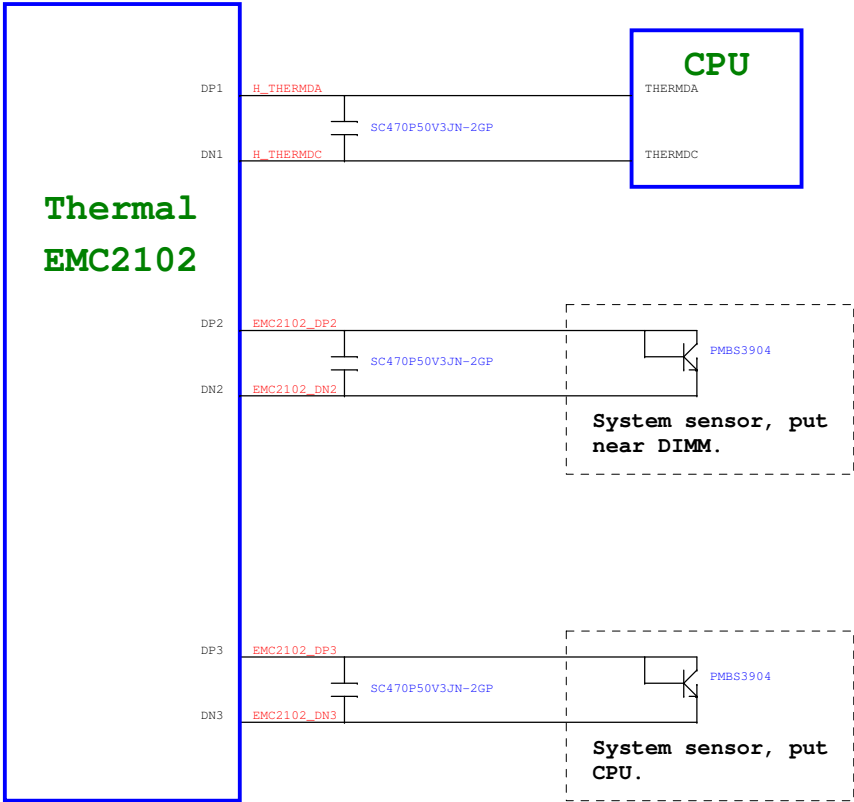
SB820M SMBus Block Diagram



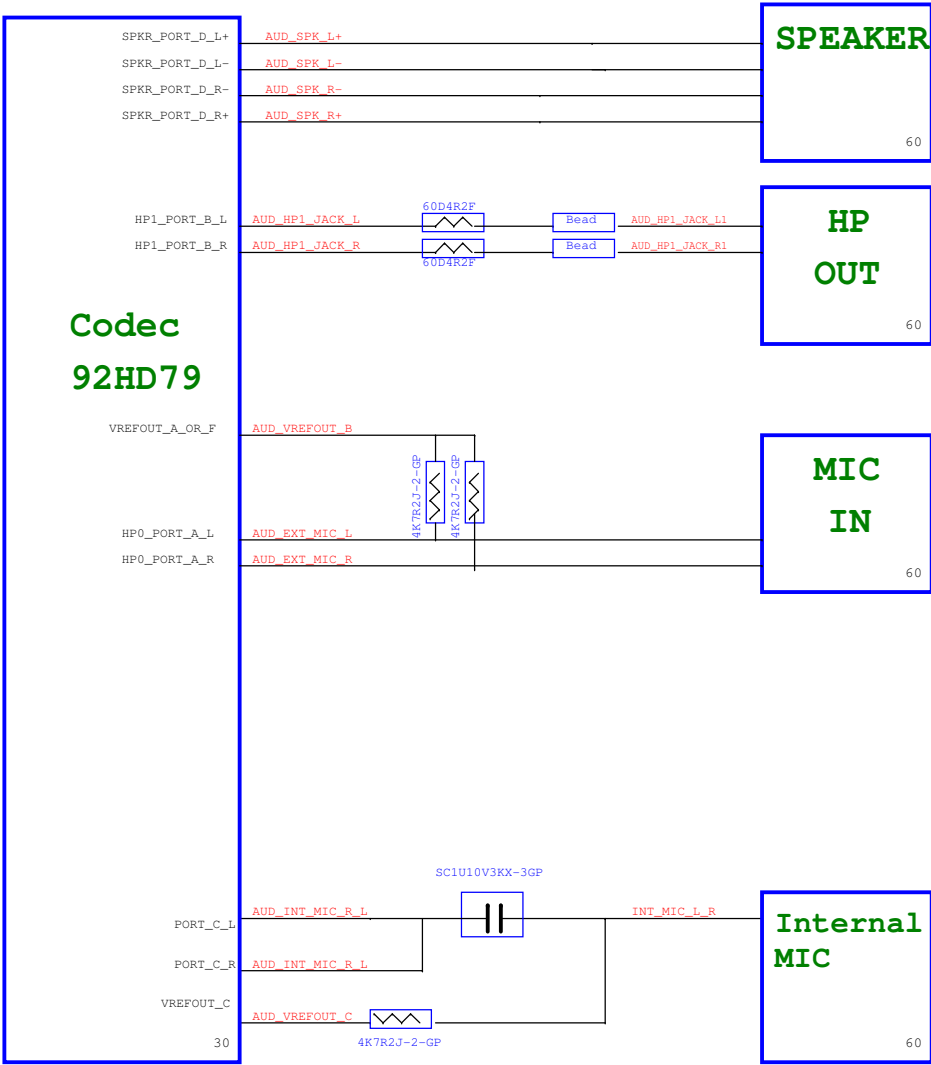
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



Capture from 45484 Rev. 1.02 AMD SB8xx-Series Southbridge Design Guide

Name	Strap Name	Schematic Note															
LPCCLK0	ECEnableStrap	Embedded Controller (EC) * 0 V - Disabled 3.3 V - Enabled															
EC_PWM3 EC_PWM2	{ROMTYPE_1, ROMTYPE_0 }	<table> <tr> <th>ROMTYPE_1</th><th>ROMTYPE_0</th><th>ROM TYPE</th></tr> <tr> <td>3.3V</td><td>0V</td><td>SPI ROM</td></tr> <tr> <td>3.3V</td><td>3.3V</td><td>Reserved</td></tr> <tr> <td>0V</td><td>0V</td><td>Firmware Hub</td></tr> <tr> <td>* 0V</td><td>3.3V</td><td>LPC ROM (supports both LPC and PMC ROM types)</td></tr> </table>	ROMTYPE_1	ROMTYPE_0	ROM TYPE	3.3V	0V	SPI ROM	3.3V	3.3V	Reserved	0V	0V	Firmware Hub	* 0V	3.3V	LPC ROM (supports both LPC and PMC ROM types)
ROMTYPE_1	ROMTYPE_0	ROM TYPE															
3.3V	0V	SPI ROM															
3.3V	3.3V	Reserved															
0V	0V	Firmware Hub															
* 0V	3.3V	LPC ROM (supports both LPC and PMC ROM types)															
LPCCLK1	CLKGEN	Defines clock generator 0V - External clock mode: Use 100-MHz PCIeR clock as reference clock and generate i nternal clocks only. * 3.3V- Integrated clock mode: Use 25-MHz crystal clock and generate both internal and external clocks															
PCICLK1	BIF_GEN2_ COMPLIANCE_Strap	Set PCIe to Gen II mode 0V- Force PCIe interface at Gen I mode * 3.3V- PCIe interface is at Gen II mode Not Applicable to SB820M but provision for pull-down is required.															
PCICLK2	BootFailTmrEn	Watchdog function * 0V- Disable the boot fail timer function 3.3V- Enable the boot fail timer function															
PCICLK3	DefaultStrapMode	Default Debug Straps * 0V- Disable Debug Straps. 3.3V- Select external Debug Straps															
PCICLK4	CPUClkSel	CPU/NB HT Clock Selection 0V- Reserved. * 3.3V- Required setting for integrated clock mode. This strap is not used if the strap CLKGEN is configured for external clock generator mode.															
AZ_SDOUT	CoreSpeedMode	Slow down core clock for low power platform. * 0V- Performance mode 3.3V- Low Power mode															

NB880M Strapping

Capture from 46113 rs880m ds_nda_1.03

Name	Strap Function	Schematic Note
DAC_VSYNC	STRAP_DEBUG_BUS_GPIO_ENABLE#	Enables debug bus access through memory I/O pads and GPIOs. 0: Enable * 1: Disable
DAC_HSYNC	SIDE_PORT_EN#	Indicates if memory side-port is available or not 0: Available * 1: Not available
SUS_STAT#	LOAD_EEPROM_STRAPS#	Selects loading of strap values from EEPROM. 0: I2C master can load strap values from EEPROM if connected, or use default values if EEPROM is not connected. Please refer to RS880M's reference schematics for system level implementation details. * 1: Use default values

USB Table

USB	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB1 (I/O Board, 17")
4	WLAN
5	Reserve
6	Reserve
7	Reserve
8	Reserve
9	Reserve
10	CARD READER
11	CAMERA
12	BLUETOOTH
13	Reserve

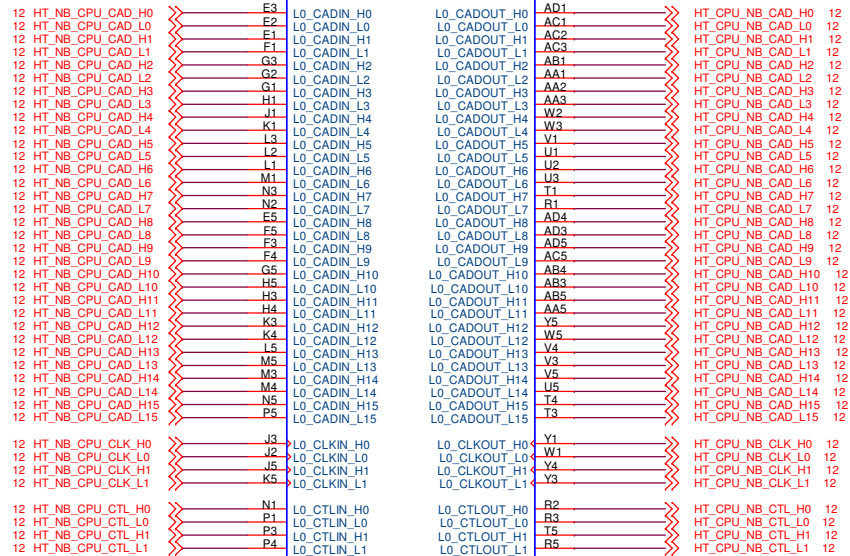
PCIe Routing

LANE0	MiniCard WLAN
LANE1	LAN

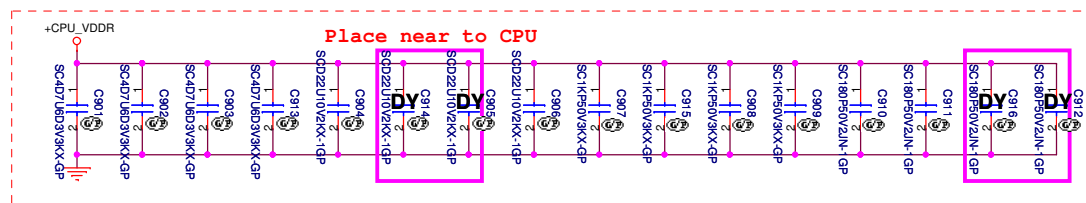
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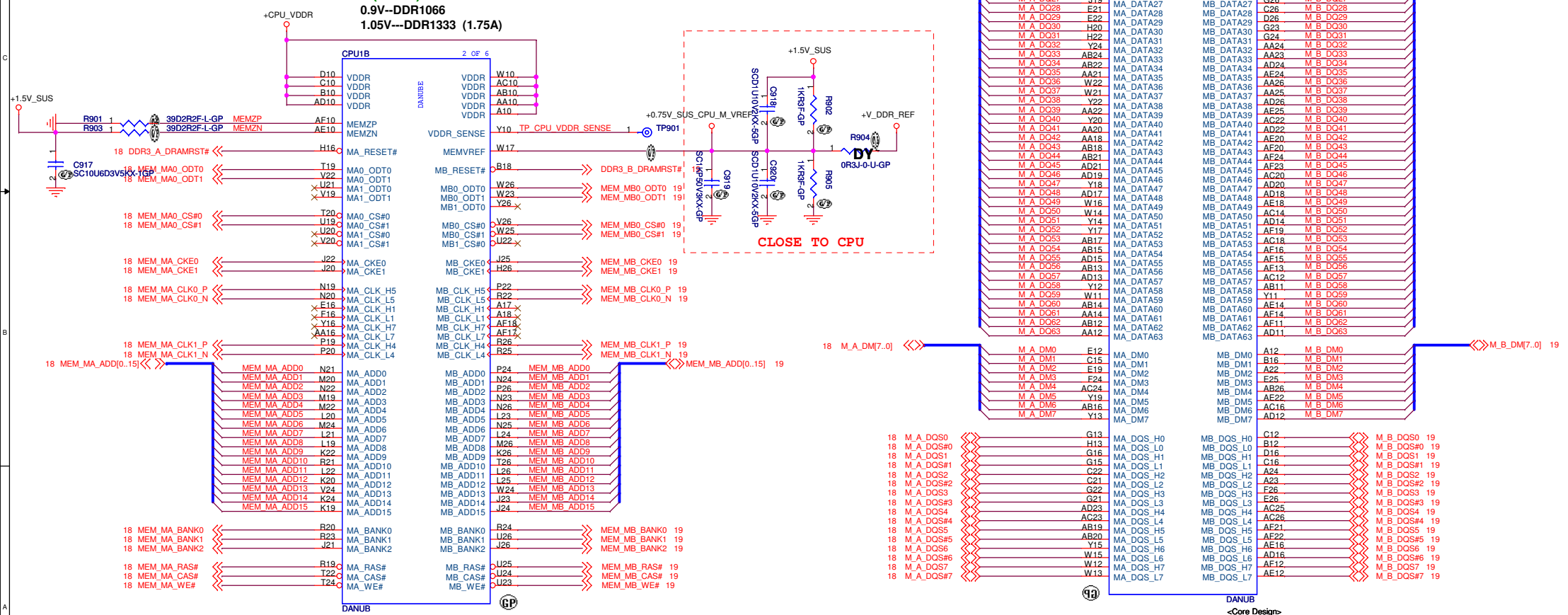
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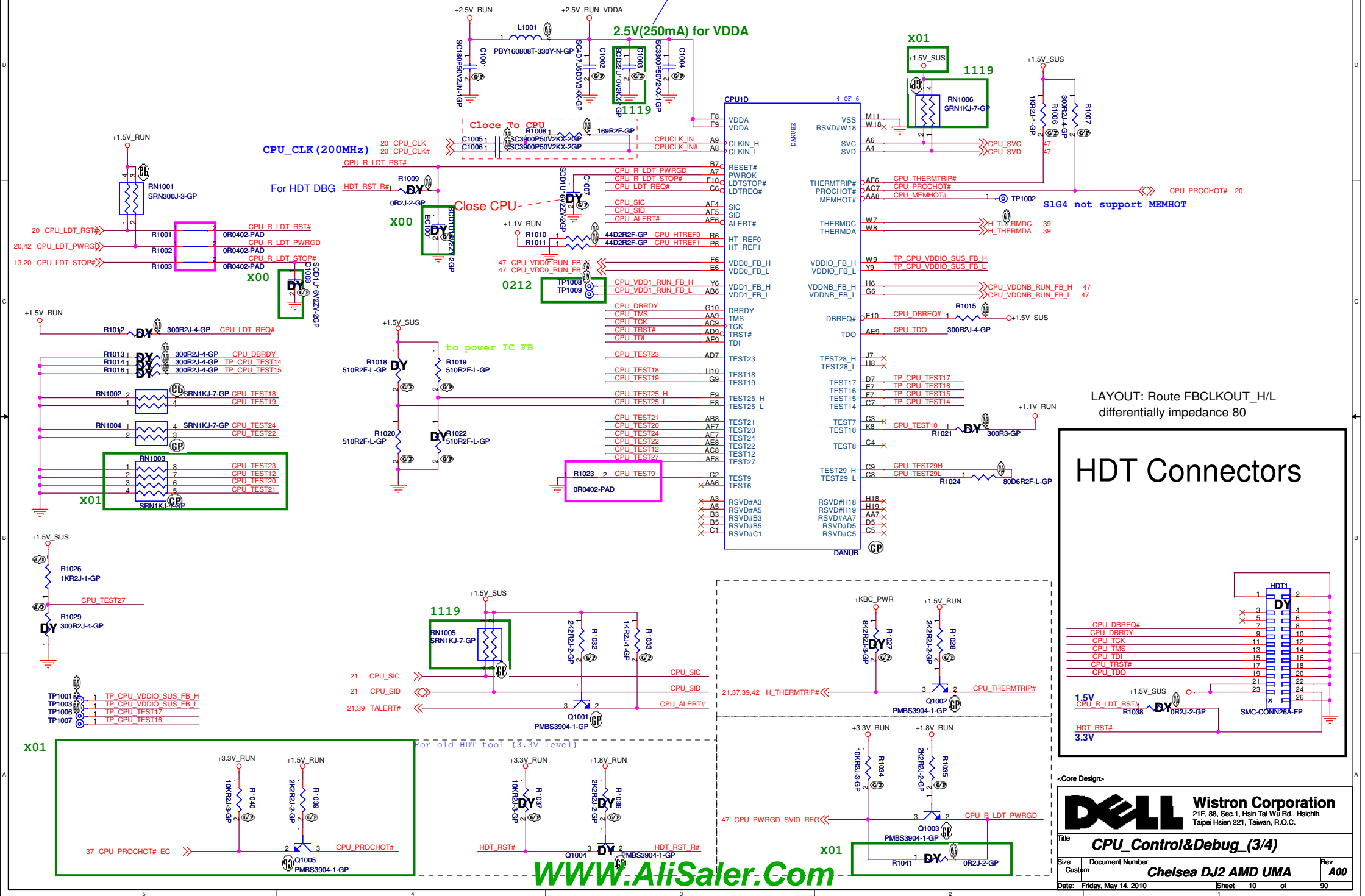
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1'nd 62.10055.111
2'nd 62.10055.181
```

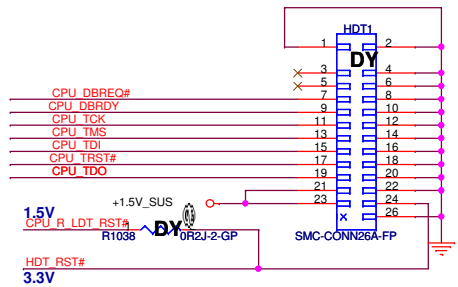
0.9V(1.25A) for VDDR
0.9V--DDR1066
1.05V---DDR1333 (1.75A)



LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD),AND 500 mils LONG.



HDT Connectors



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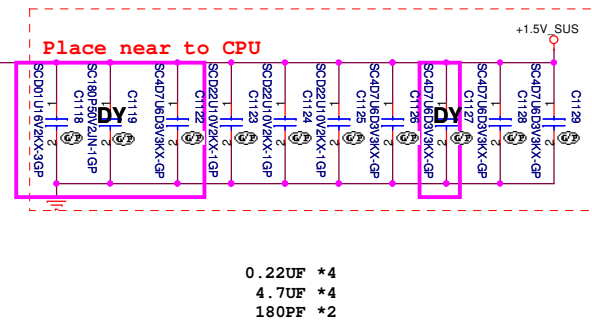
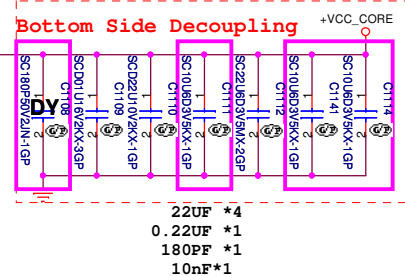
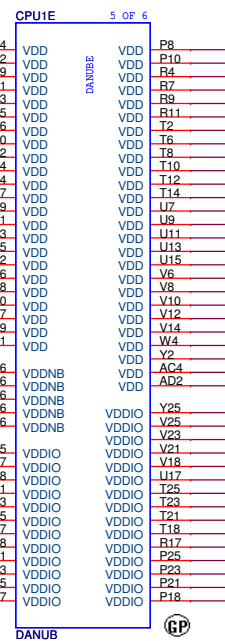
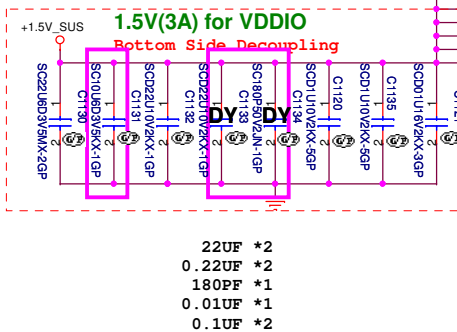
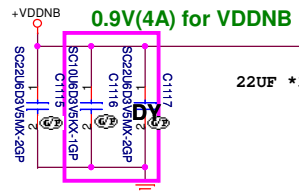
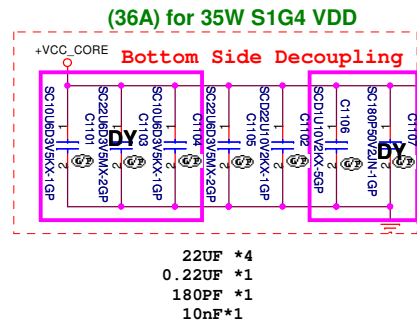
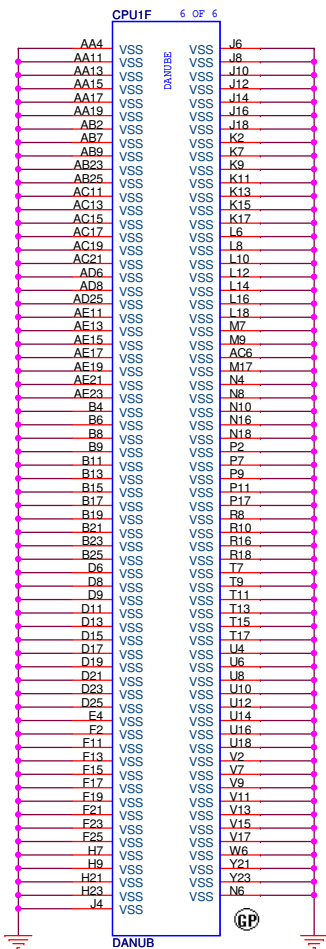


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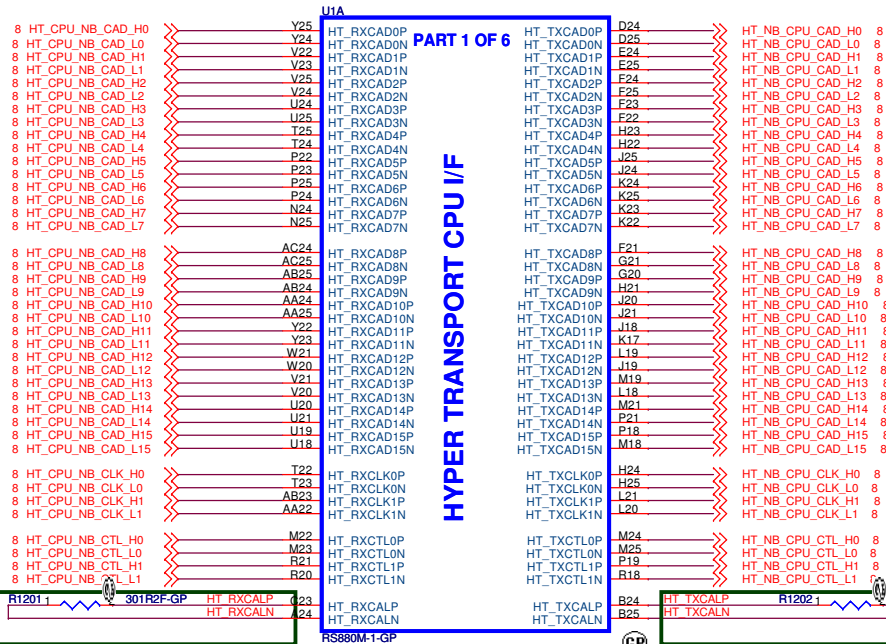
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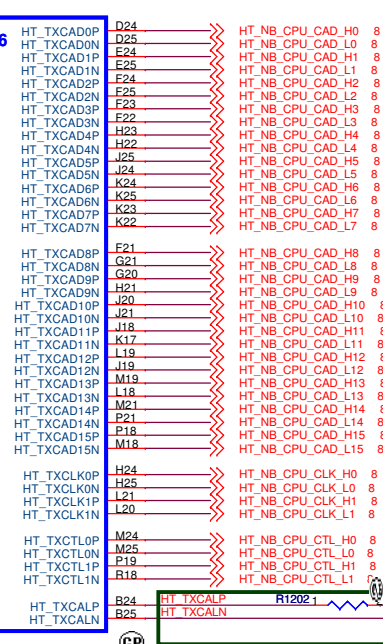
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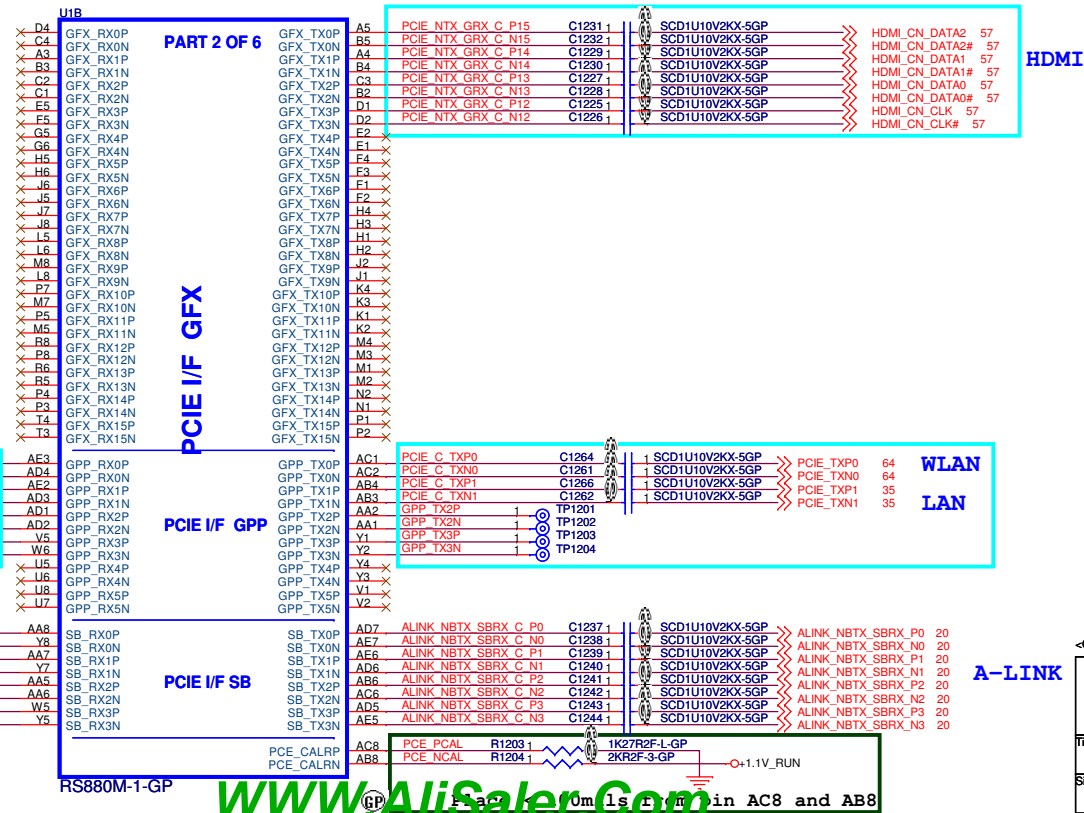
RS880M : 71.RS880.M05



```
Place < 1000mils from pin C23 and A24
```



GP Place < 1000mils from pin B25 and B24



HDMI

A-LINK

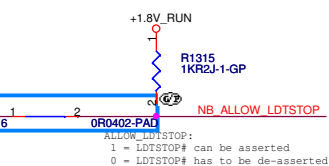
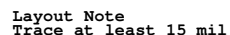
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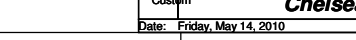
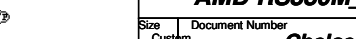
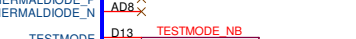
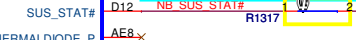
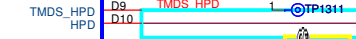
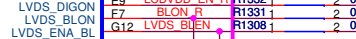
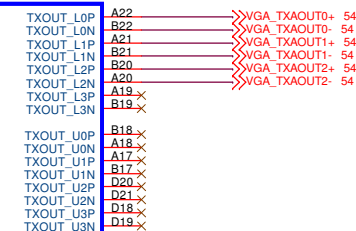
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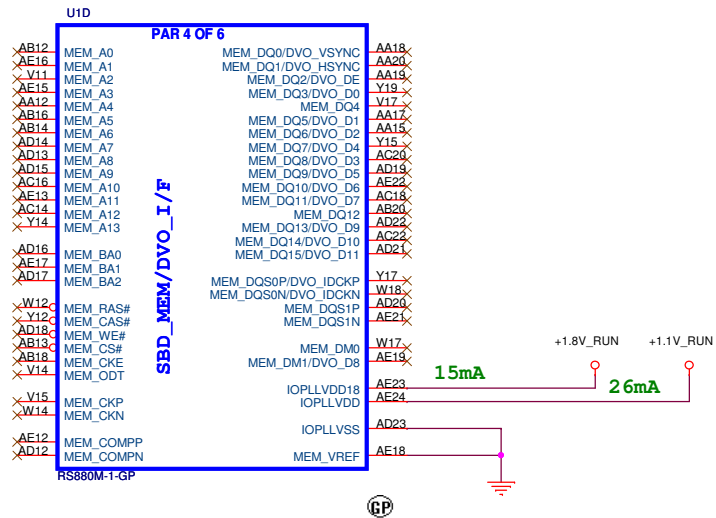
+1.1V_RUN



*DEFAULT




SSID = N.B





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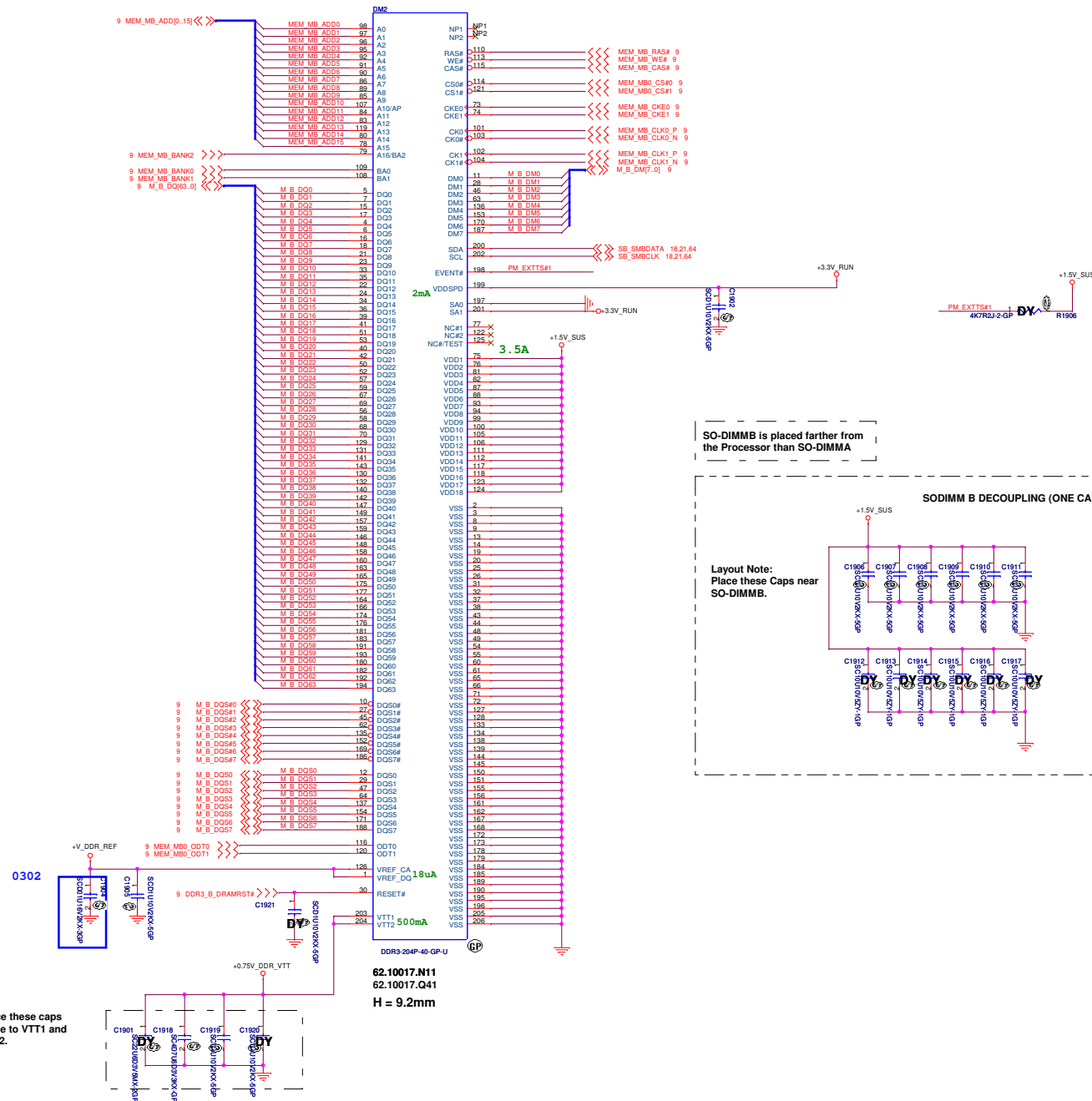
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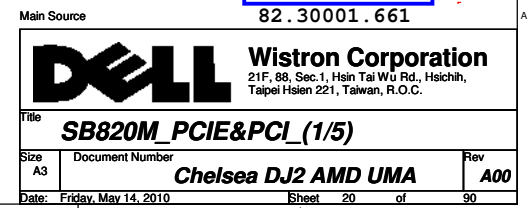
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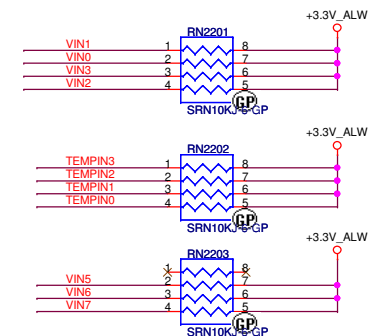
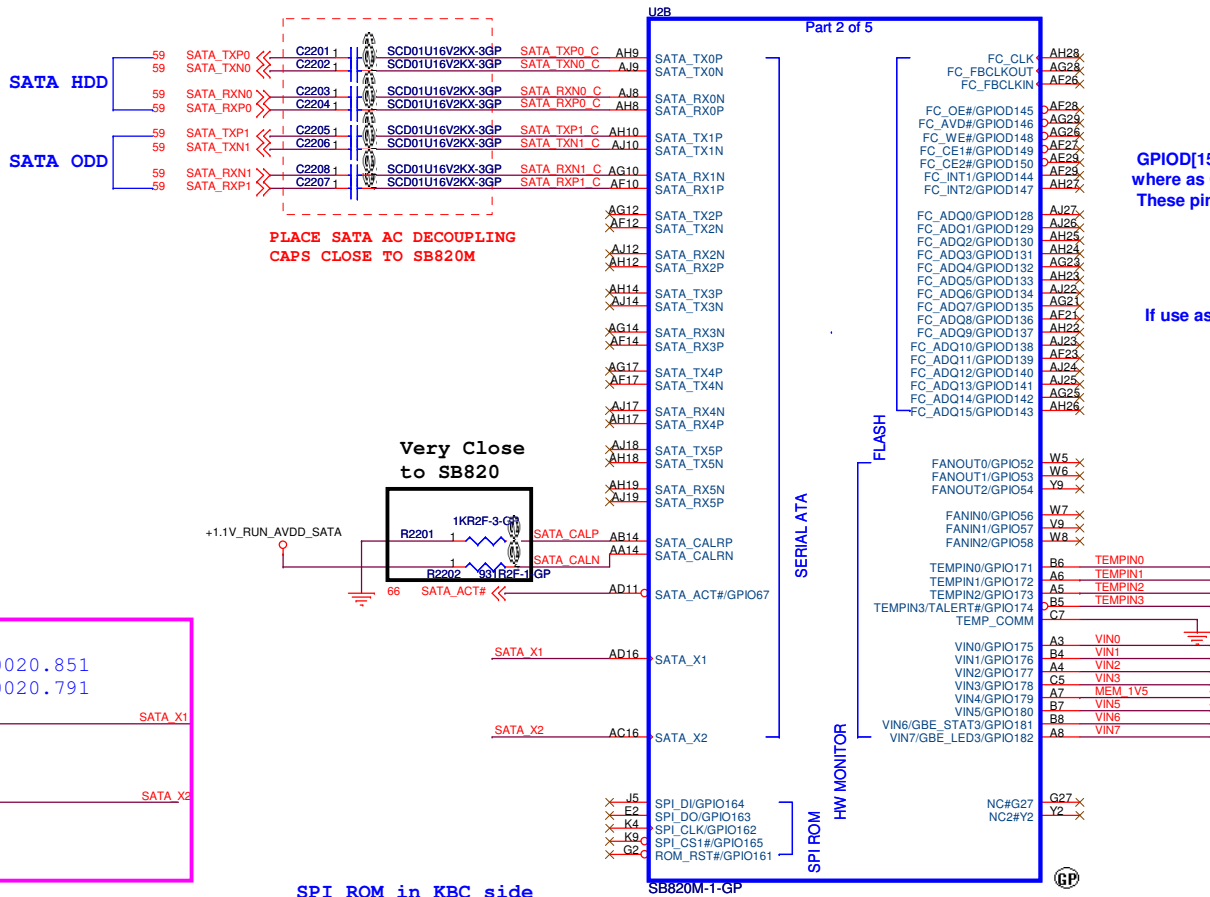
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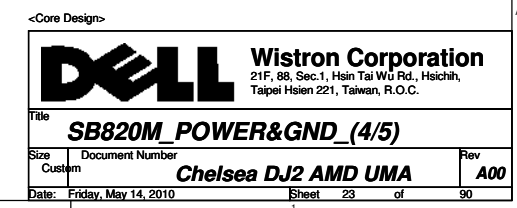
PCI_CLK3



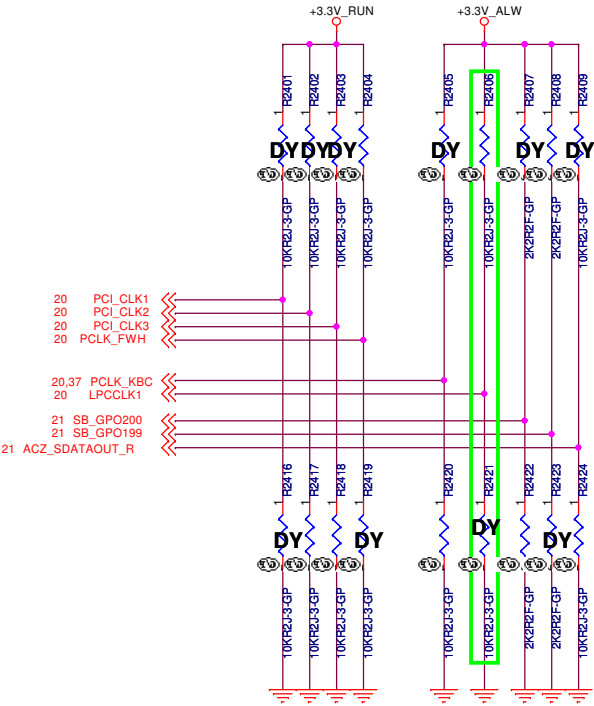
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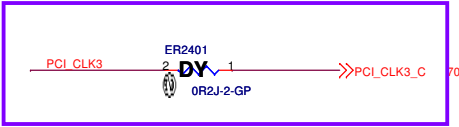




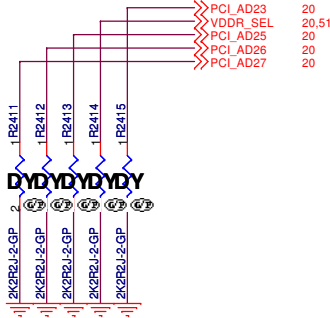
REQUIRED STRAPS



-A00



DEBUG STRAPS



REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCLK_FWH (PCI_CLK4)	PCLK_KBC (LPCCLK0)	LPCCLK1	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	DEFAULT CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	L, H = LPC ROM L, L = FWH ROM


Not Applicable to SB820M but provision for pull-down is required.

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

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CPU (VCC CORE)

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CPU (VCC_GFXCORE)

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CPU (VSS)

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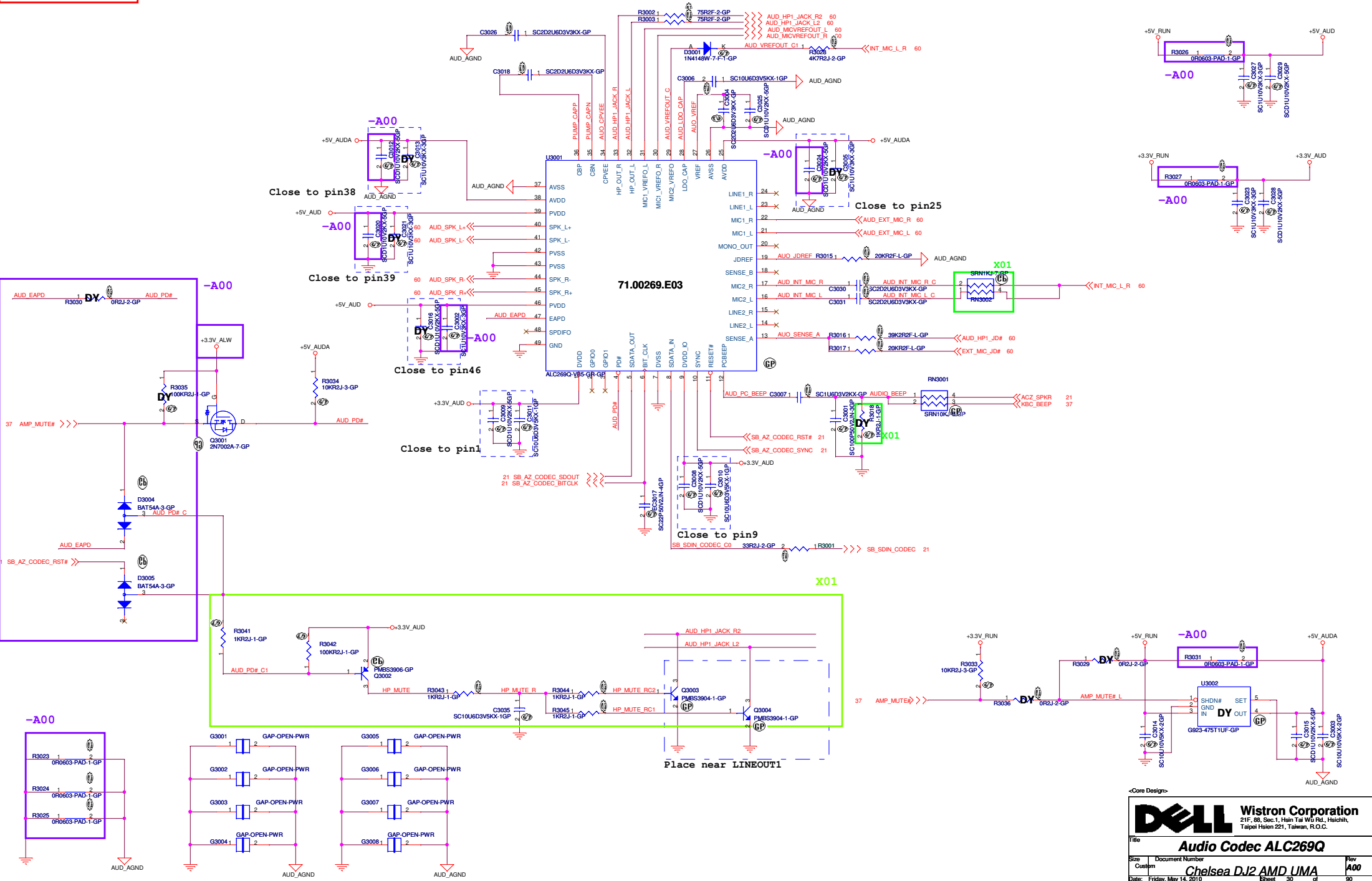
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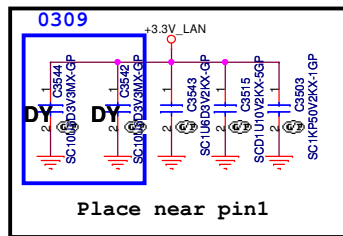
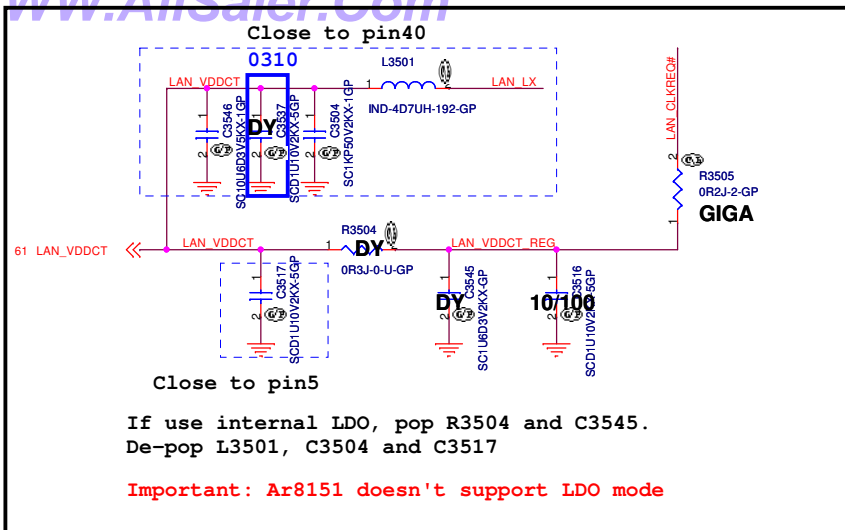
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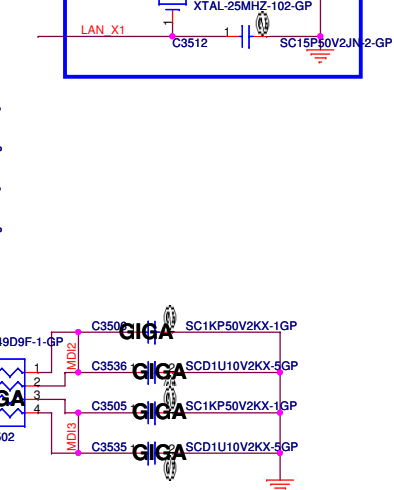
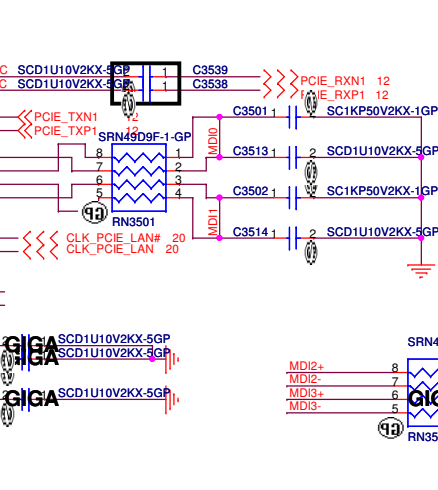
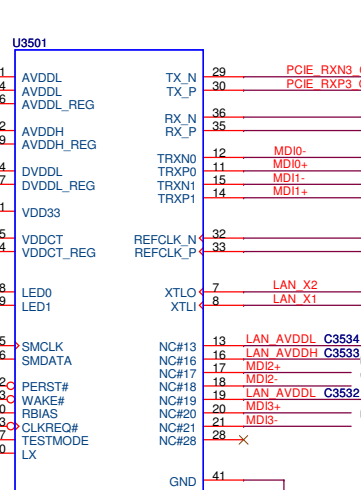
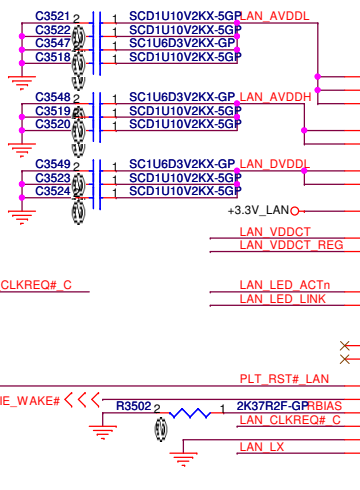
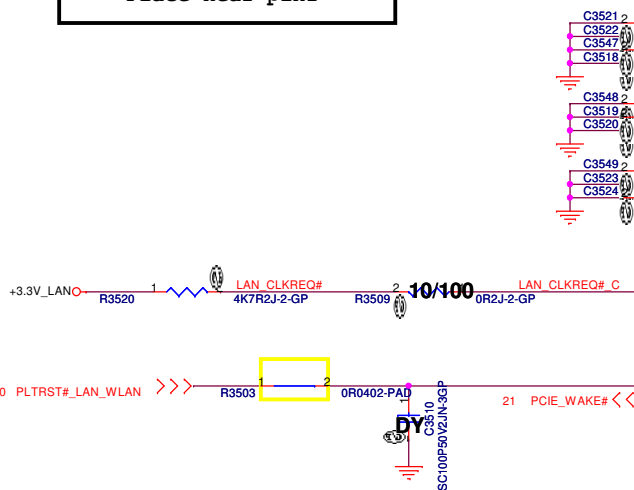
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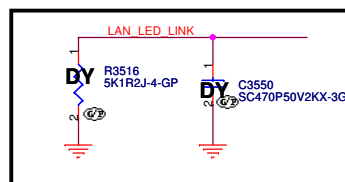
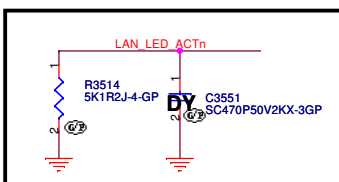
Pin6 is the AVDDL LDO output, 1uF+0.1uF (C3547 and C3518) close to Pin6;
C3522, C3521 close to Pin31, Pin34 respectively.
Pin9 is the AVDDH LDO output, 1uF+0.1uF (C3548 and C3519) close to Pin9;
C3520 close to Pin22.
Pin37 is the DVDDL LDO output, 1uF+0.1uF (C3549 and C3523) close to Pin37;
C3524 close to Pin24.



If overclocking, de-pop R3514 and C3551


If use LDO mode, pop R3516 and C3550

GIGA LAN use 71.08151.003



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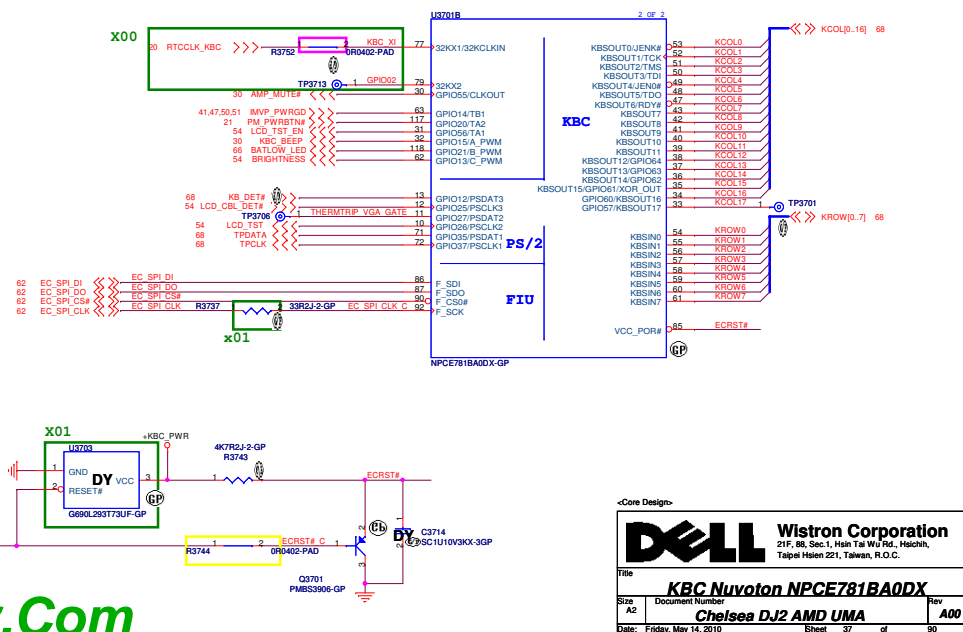
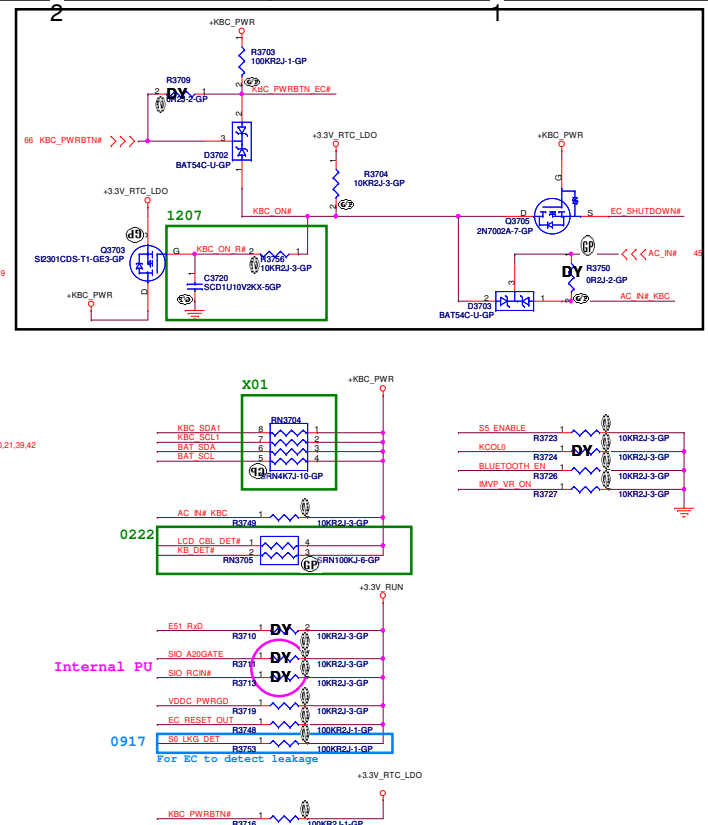
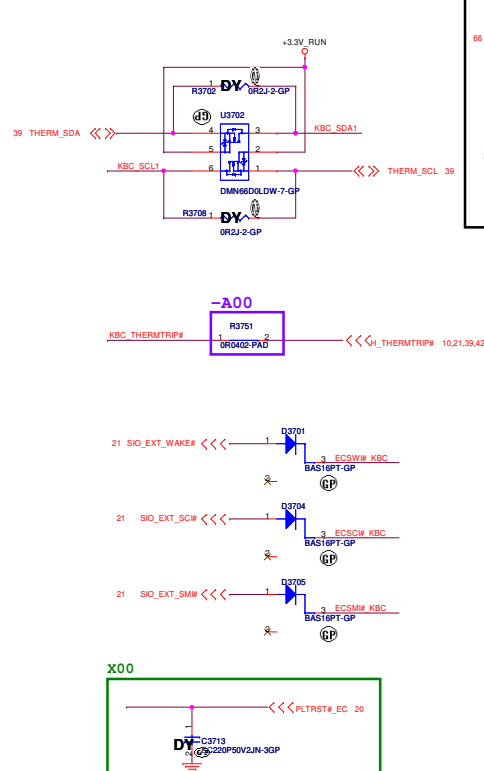
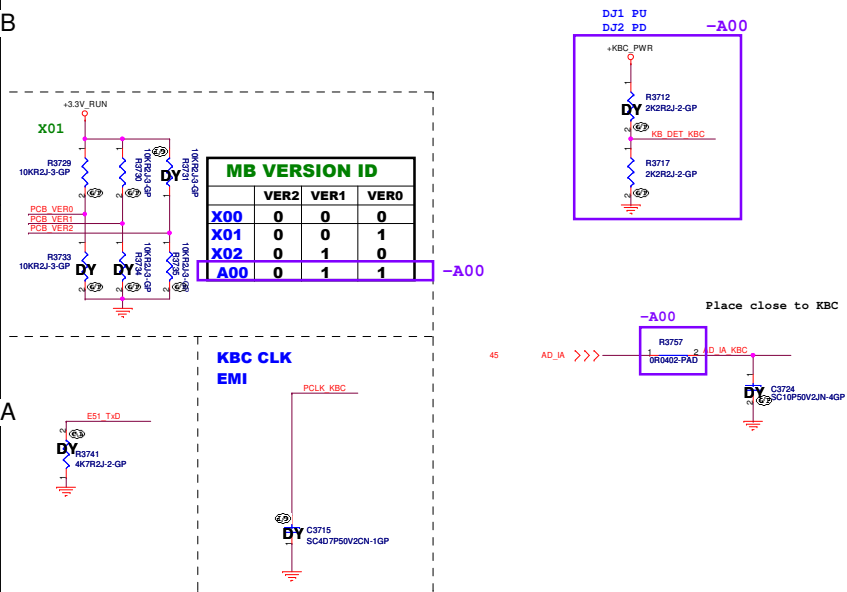
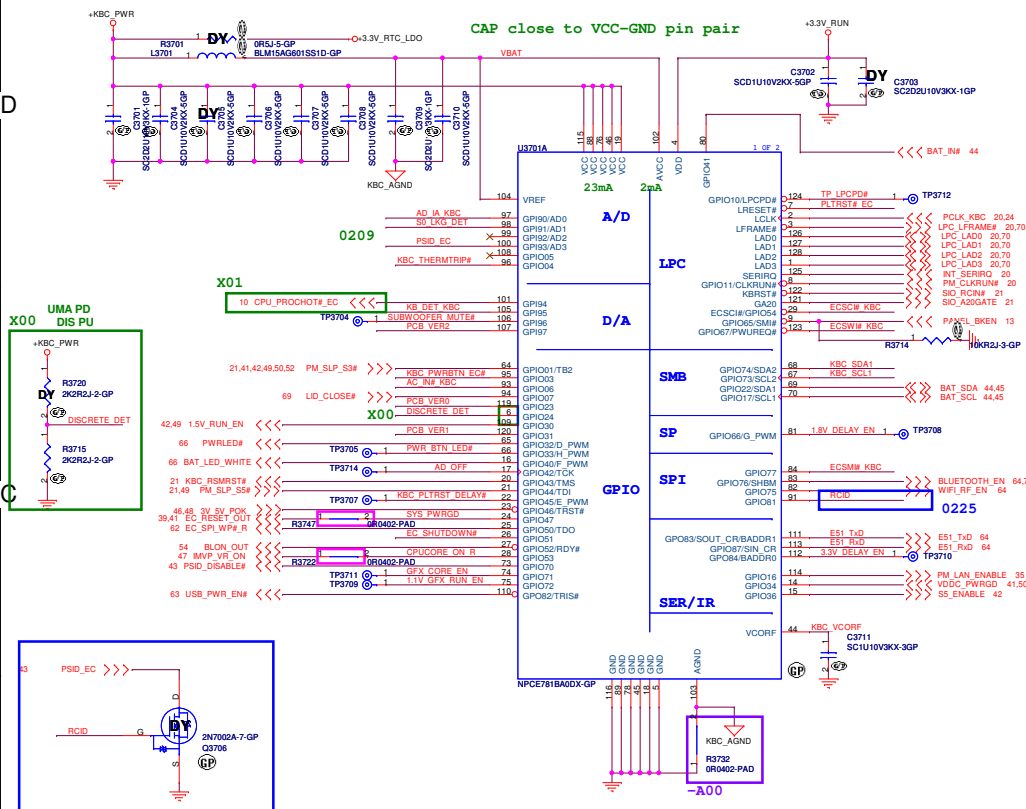
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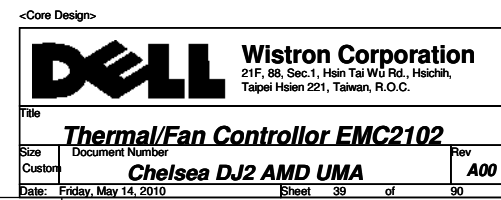
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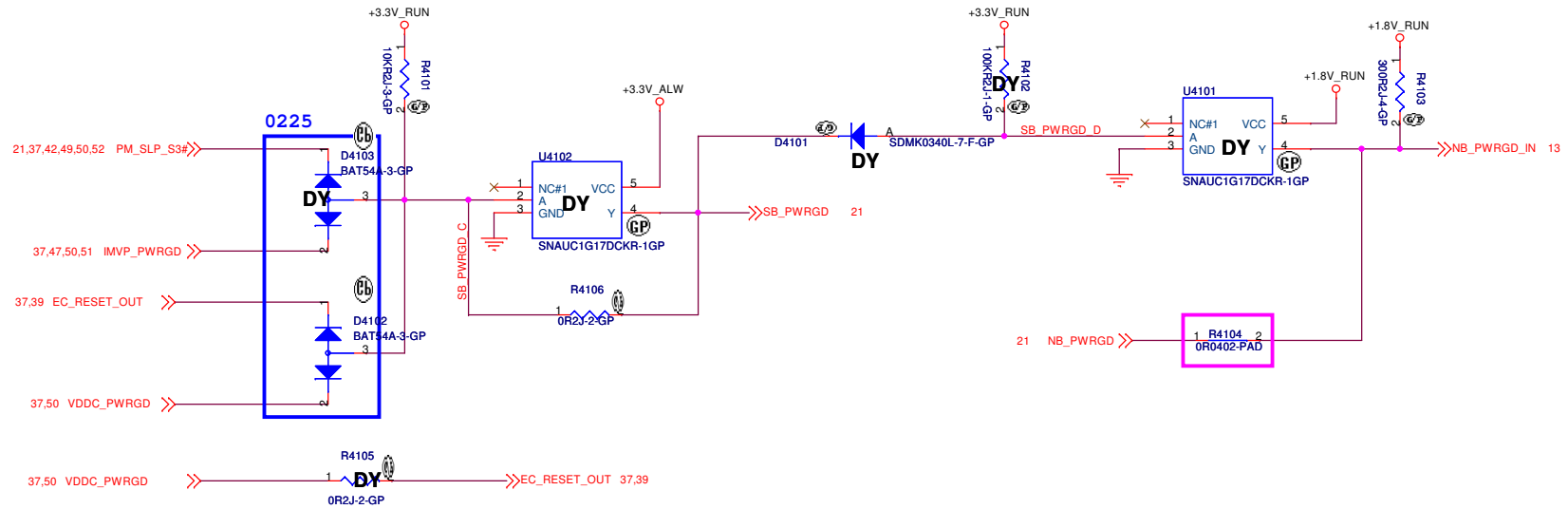
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

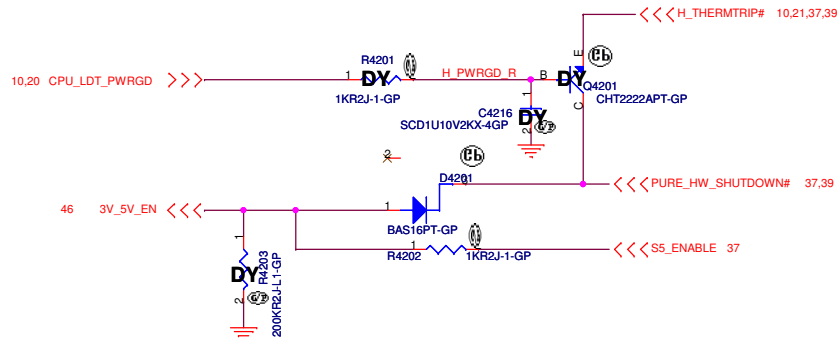
Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	A00
Date:	Friday, May 14, 2010	Sheet 40 of 90

SSID = Reset.Suspend

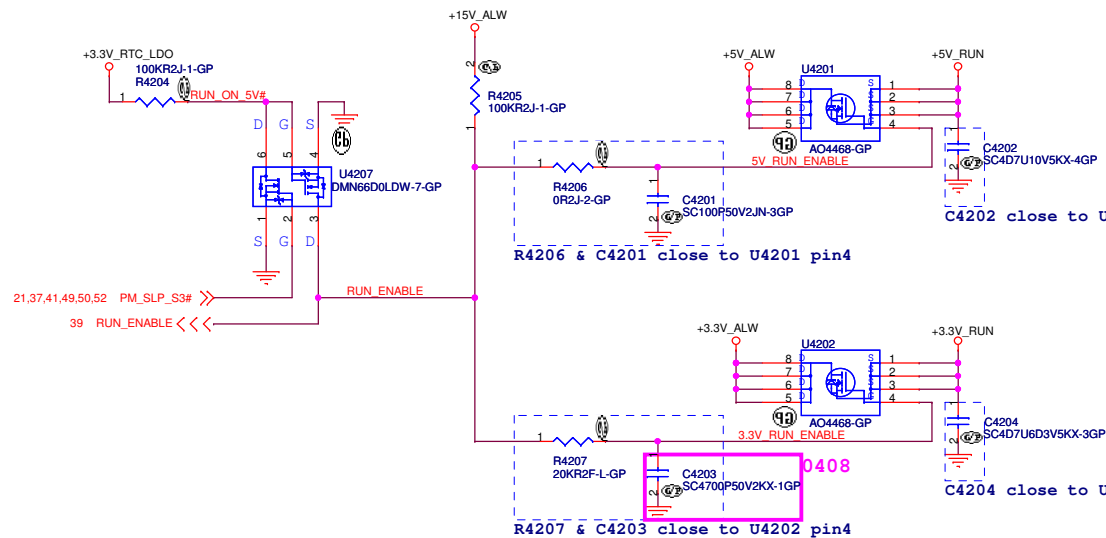


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DELL		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Power On Logic			
Size A3	Document Number Chelsea DJ2 AMD UMA	Rev A00	
Date: Friday, May 14, 2010	Sheet 41	of 90	

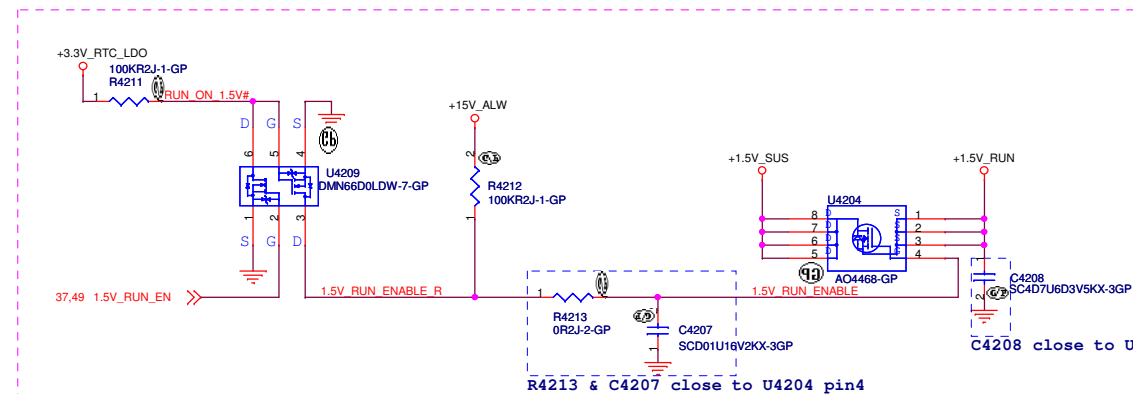


Run Power

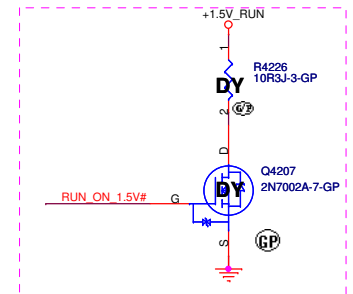


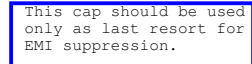
Peak current: 6257.3mA (HD:1100 ODD:2500)
Design current: 4380.11 mA
11.6A
Rds=14m ohm

Peak current: 5966mA
Design current: 4177 mA
11.6A
Rds=14m ohm



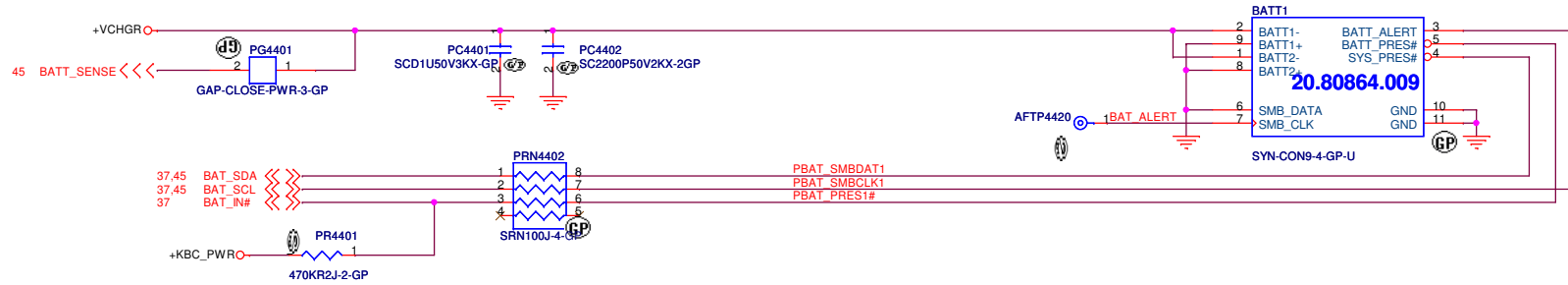
Peak current: 1230mA
Design current: 861 mA
11.6A
Rds=14m ohm



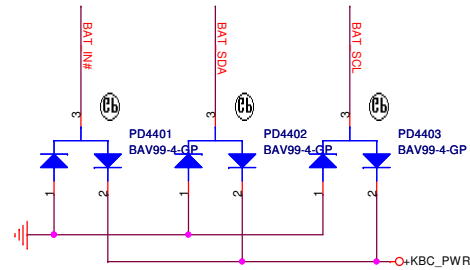
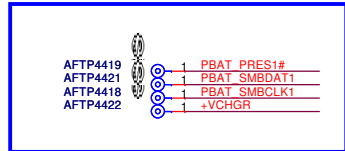


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Batt Connector

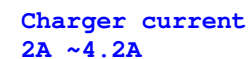


0303



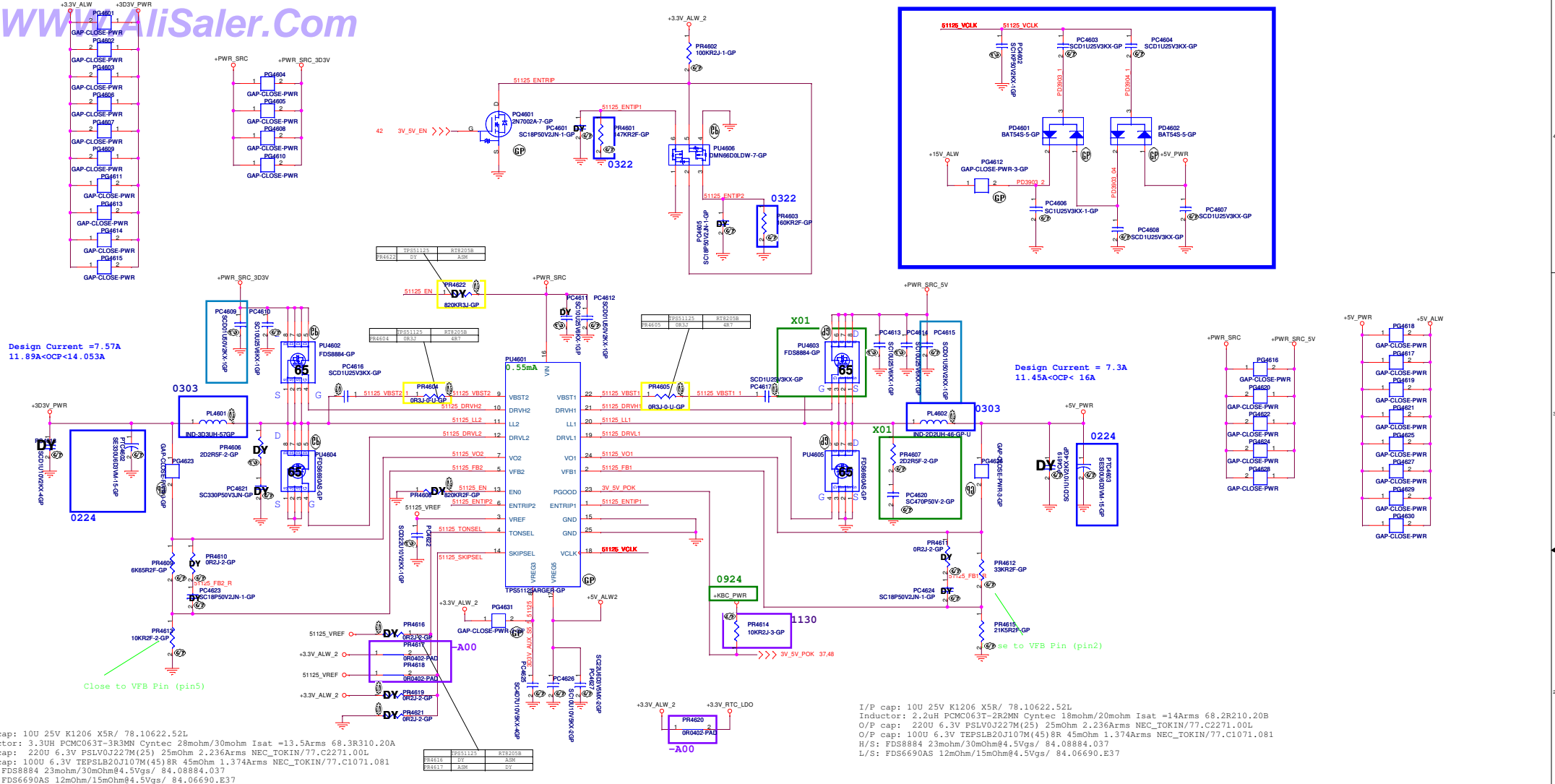
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DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
BATT CONN			
Size A3	Document Number Chelsea DJ2 AMD UMA	Rev A00	
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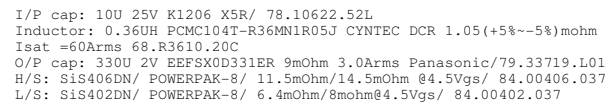
TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

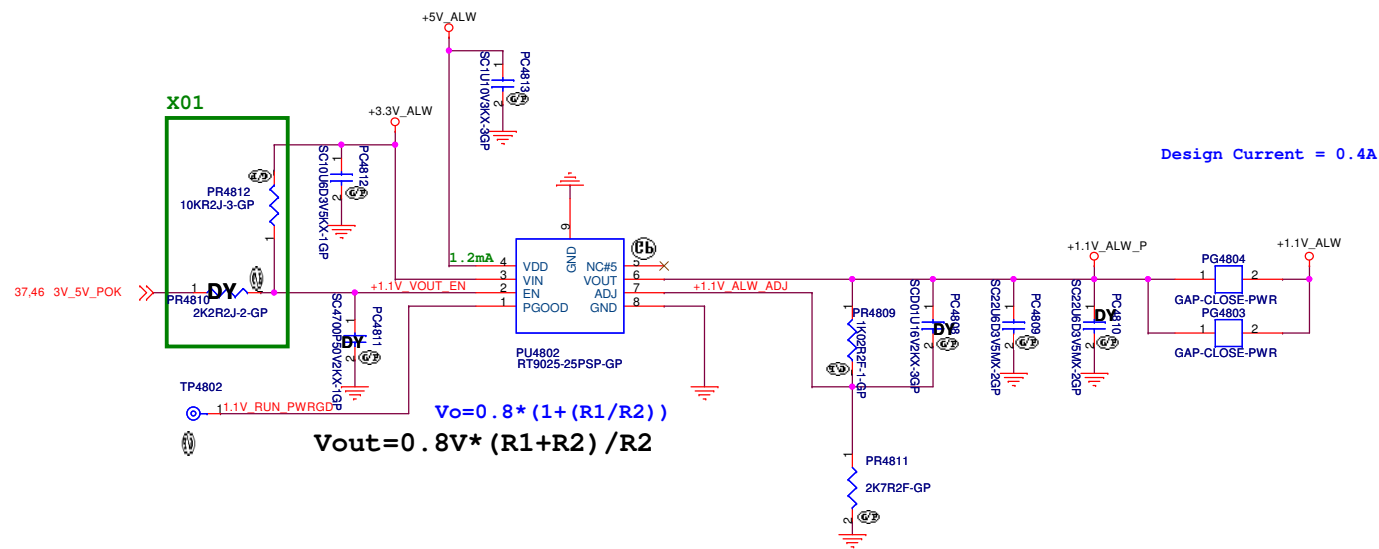
TPS51125	74.51125.073
RT8205BGQW	74.08205.B73

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

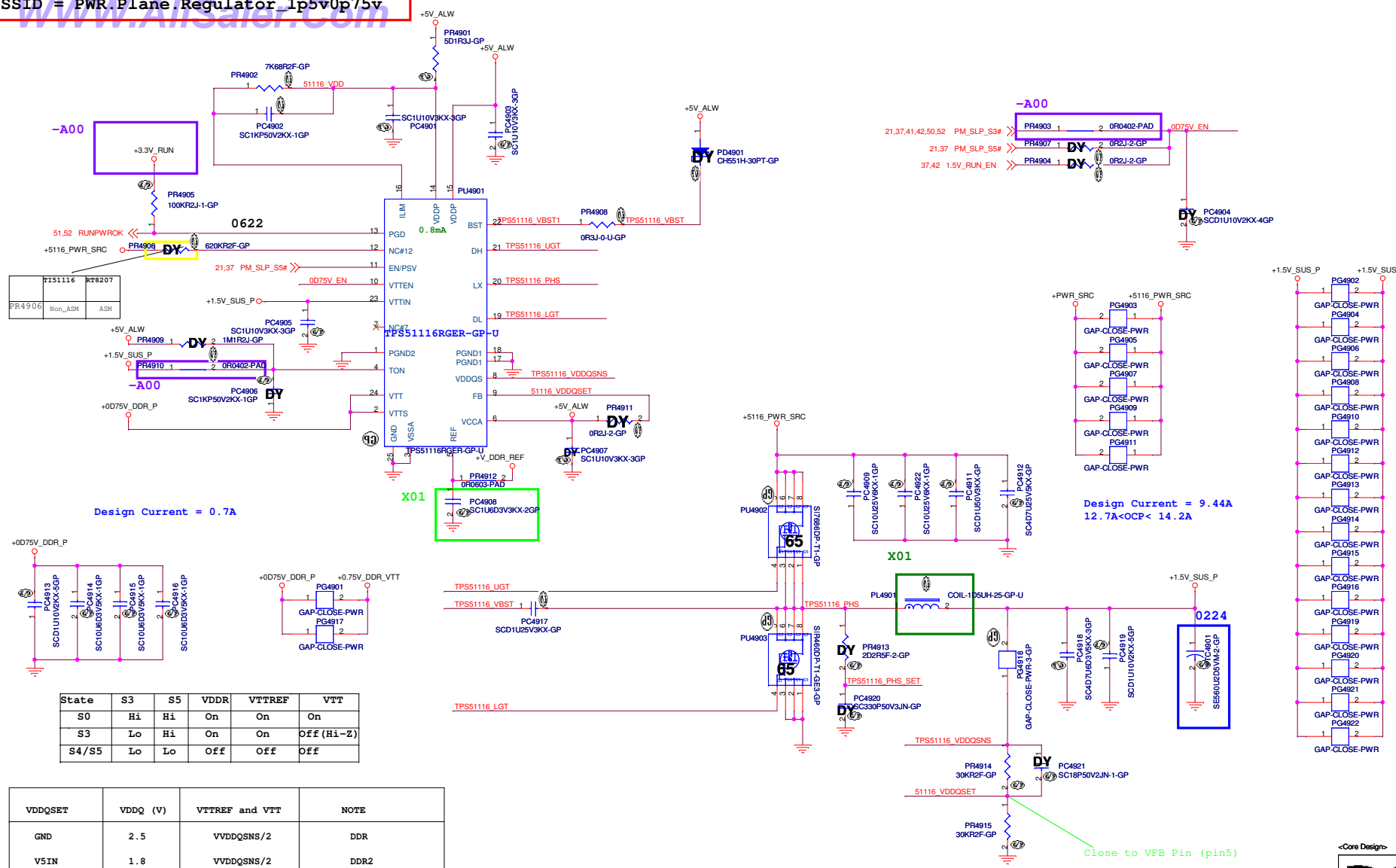
EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit



RT9025 for +1.1V_ALW




```
SSID = PWR.Plane.Regulator_1p5v0p75v
```



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

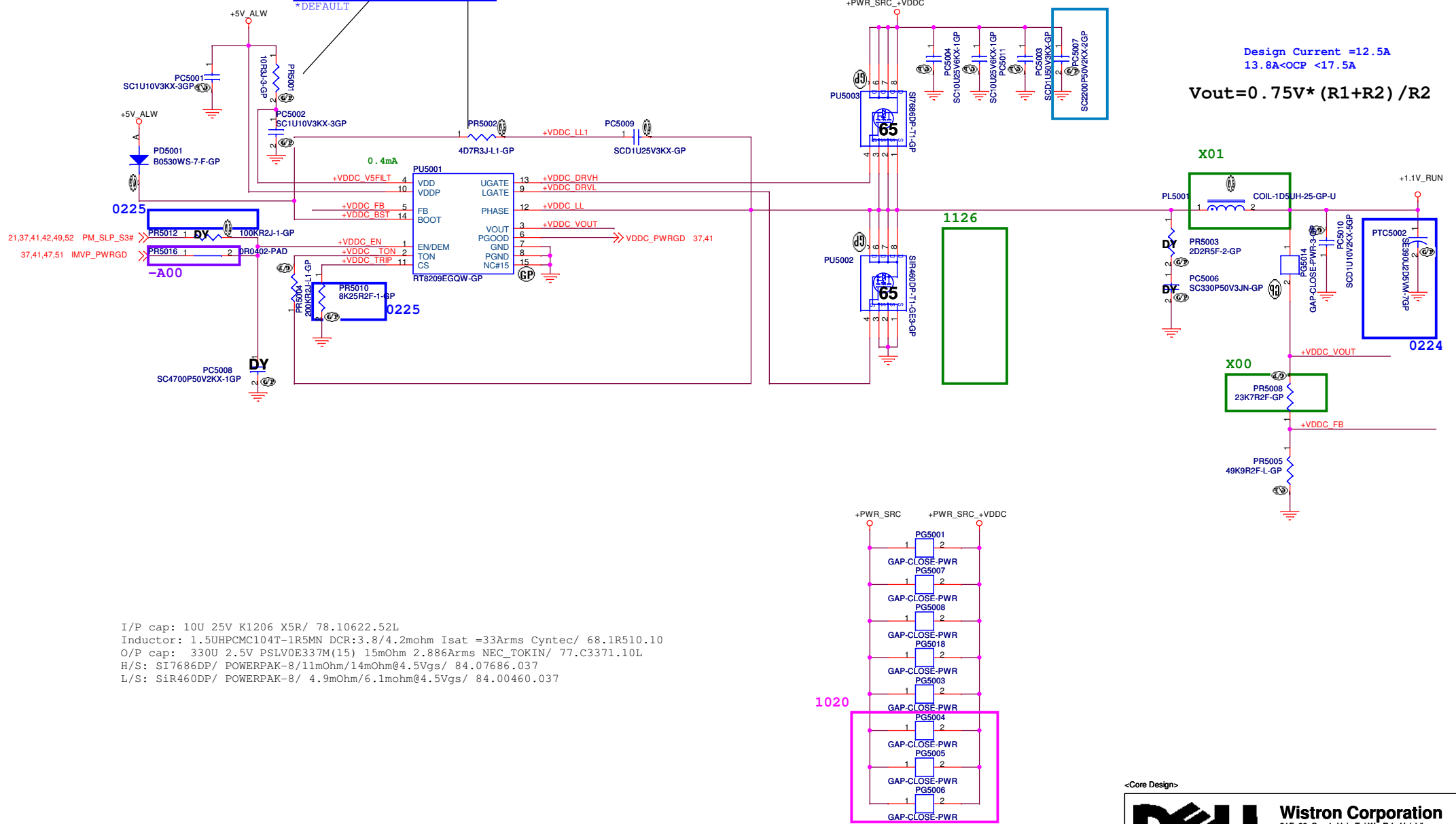
VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VDDQD < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5M1 DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10J
O/P cap: 220U 2V EEFX0D221R 15mohm 2.7Arms PANASONIC/ 79.22719.20L
H/S: FDS8880 9.6mohm/12mohm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS 5.9mohm/7.25mohm@4.5Vgs/ 84.06676.A37

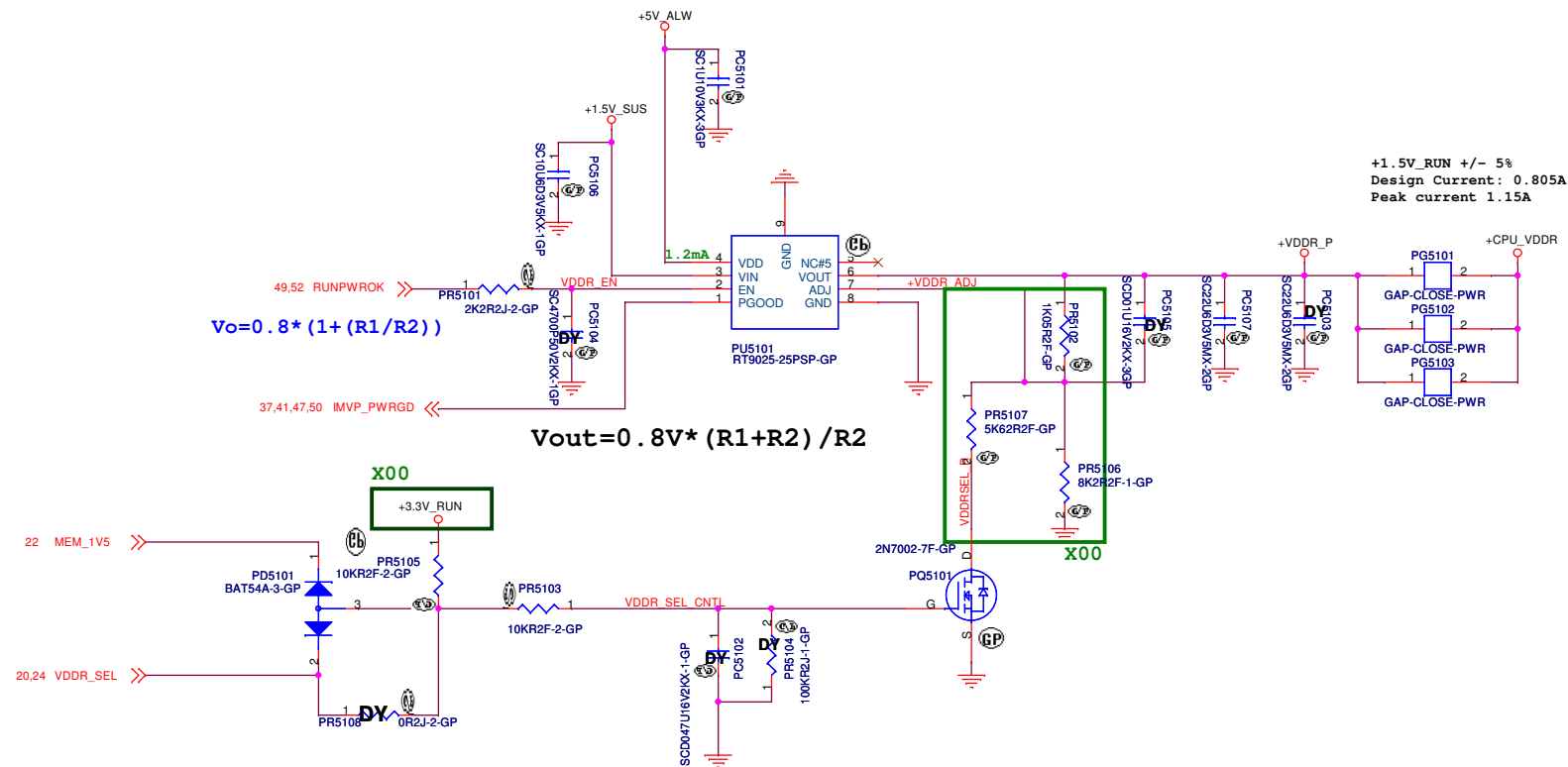
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File# _____	
<i>TPS51116RGER +1.5V SUS</i>	
Size _____ Custom _____	Document Number _____ <i>Chelsa D2 AMD UMA</i>
Date: _____ (Friday, May 14, 2006)	Sheet 49 of 90 <i>A00</i>

PWM TYPE	PR5001	PR5002
*RT8209E	10 ohm	4.7 ohm
TPS51117	300 ohm	0 ohm

*DEFAULT



RT9025 for +VDDR



VDDR_SEL	+CPU_VDDR
H	1.05V
L	0.9V

<Core Design>



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1	Title	Date	Page
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RT9025 +VDDRSize
A3

Document Number	
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Chelsea DJ2 AMD UMA

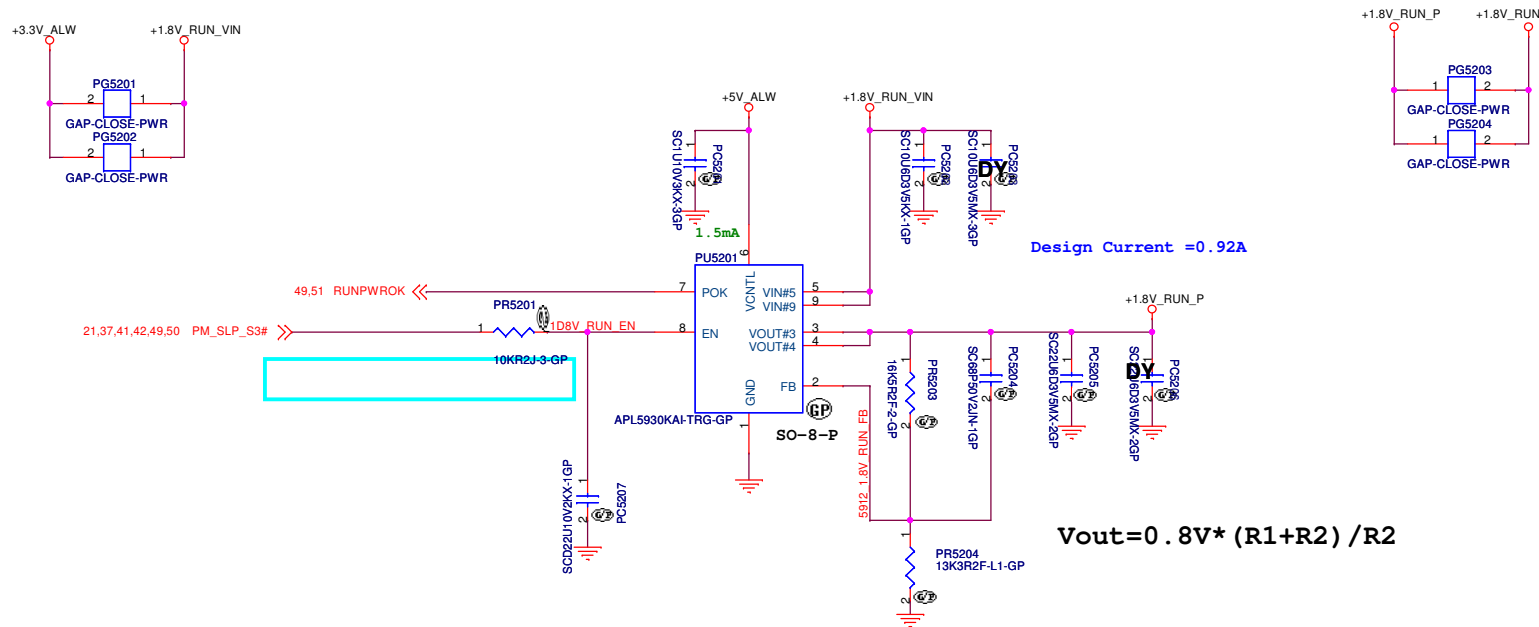
Rev
A00

Date: Friday, May 14, 2010

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SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



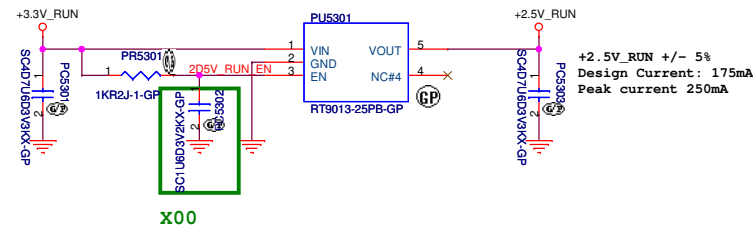
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DELL Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title APL5930 +1.8V_RUN		
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WWW.AliSaler.Com

SSID = PWR.Plane.Regulator_2p5v

RT9013-25PB for +2.5V_RUN



<Core Design>

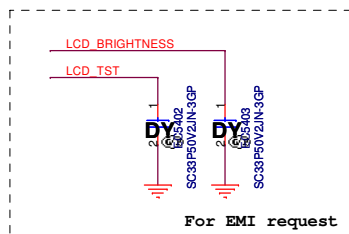
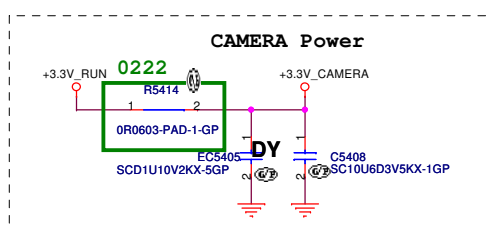
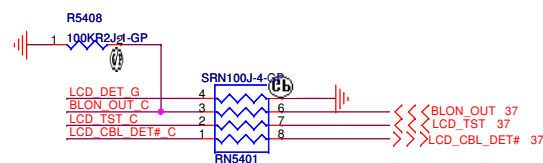
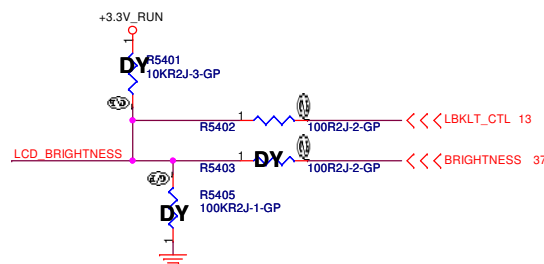
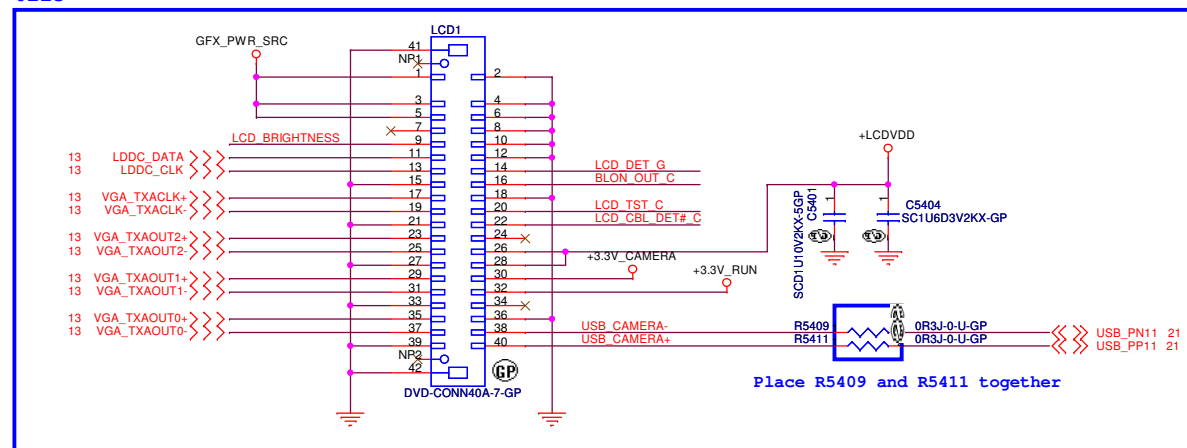


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Title			VREG : +CPU_VDDR&+2.5V_RUN		
Size	Document Number	Rev			
Custom	Chelsea DJ2 AMD UMA			A00	
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LVDS CONNECTOR

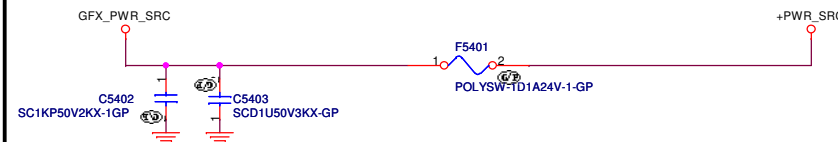
0225



For EMI request

SSID = Inverter

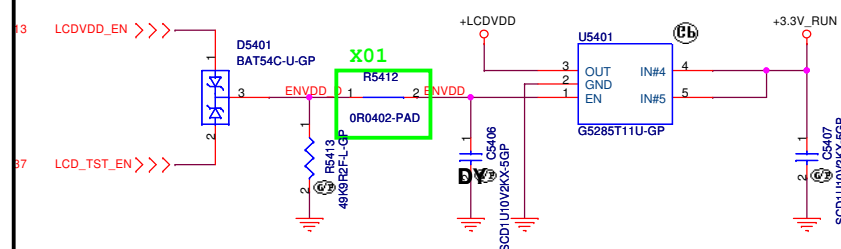
INVERTER POWER



0224

SSID = VIDEO

LCD POWER



<Core Design>

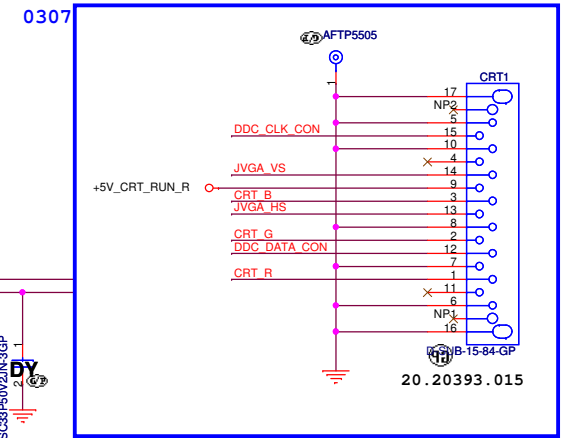
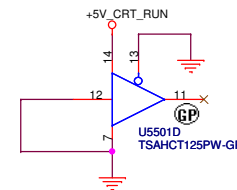
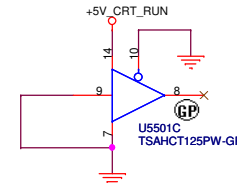
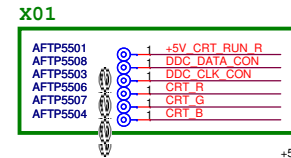
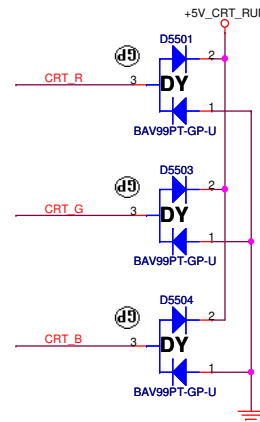
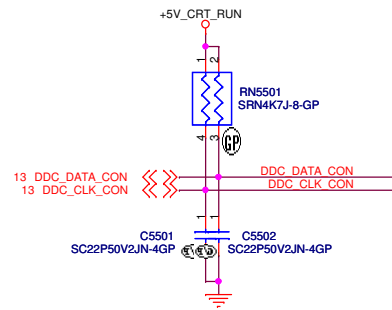
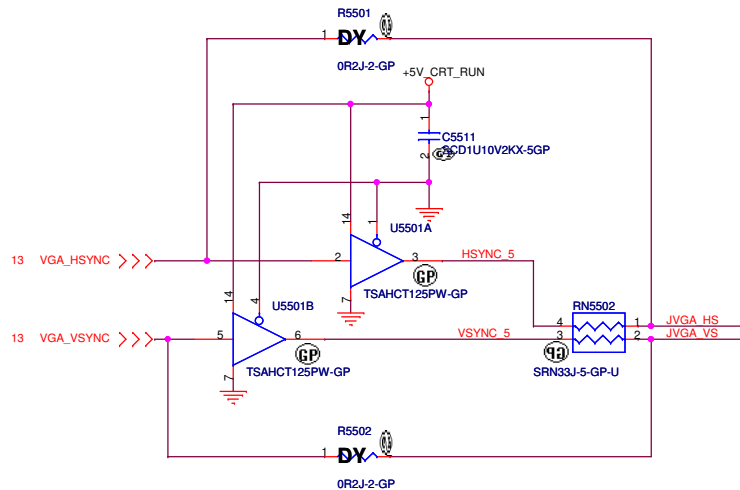
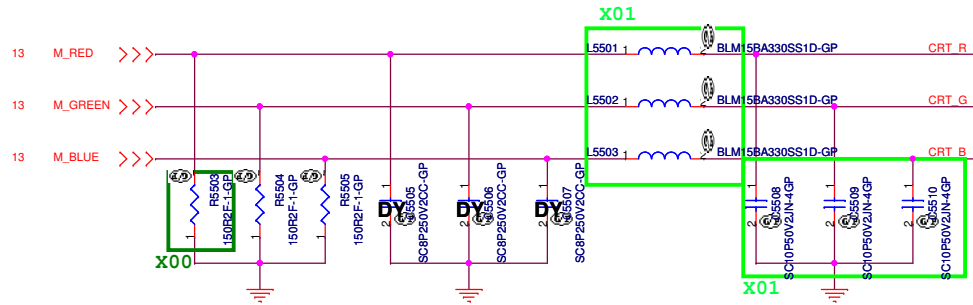
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

LCD/Inverter Connector			
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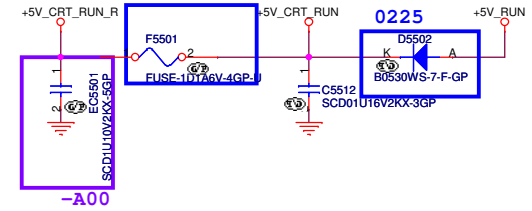
SSID = VIDEO

Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



69.50007.691




<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
CRT Connector					
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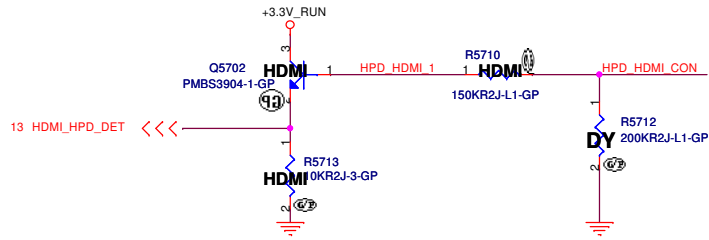
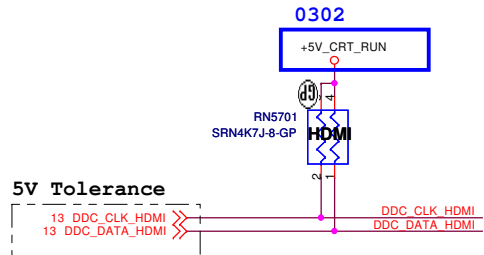
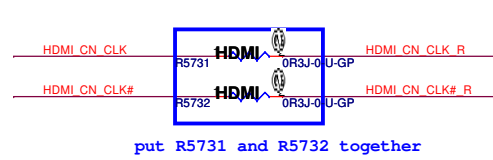
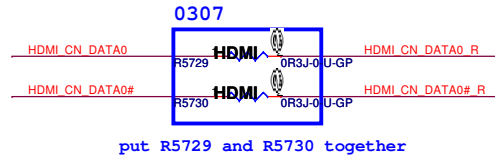
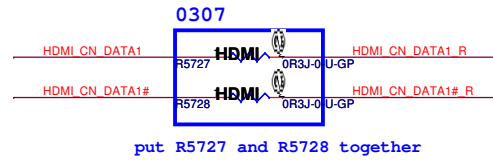
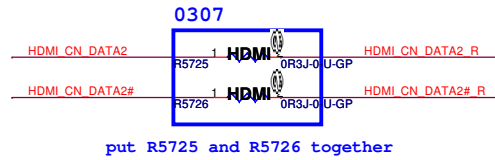
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

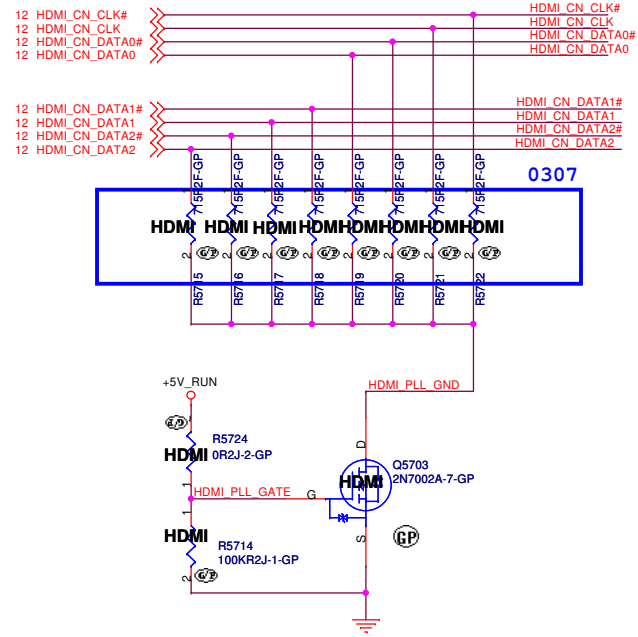
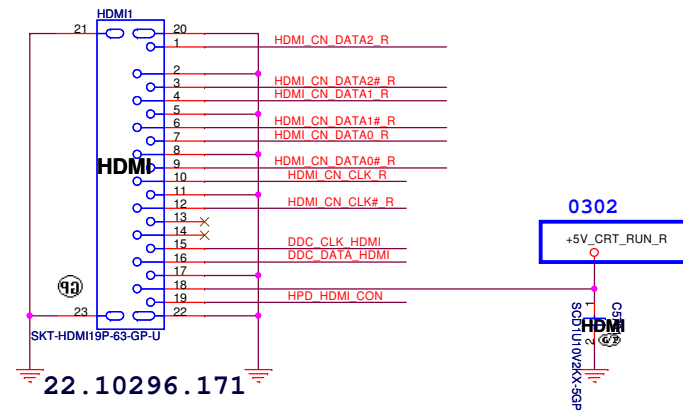
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Size A3	Document Number Chelsea DJ2 AMD UMA	Rev A00
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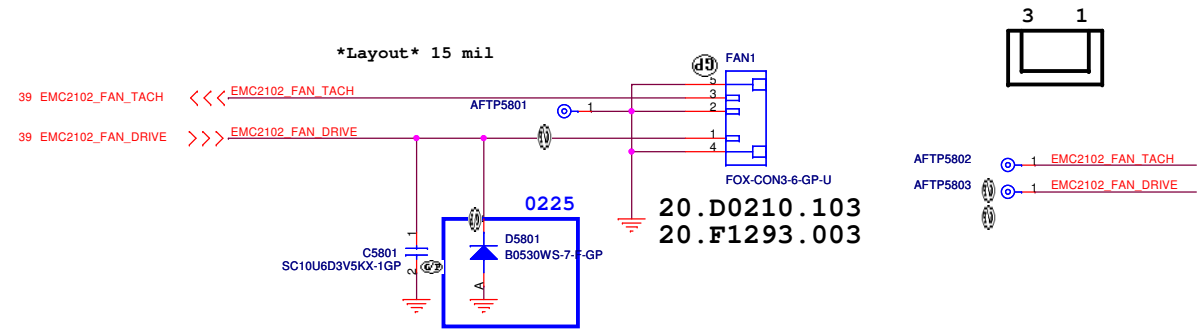
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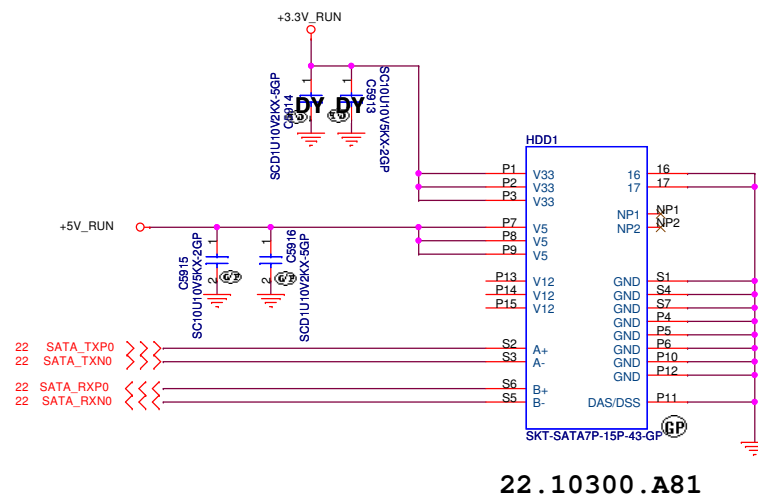
HDMI CONN



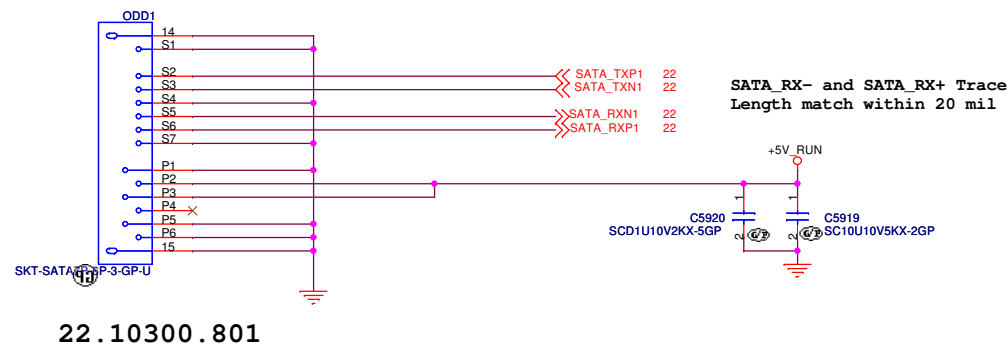
Fan Connector



SATA HDD Connector

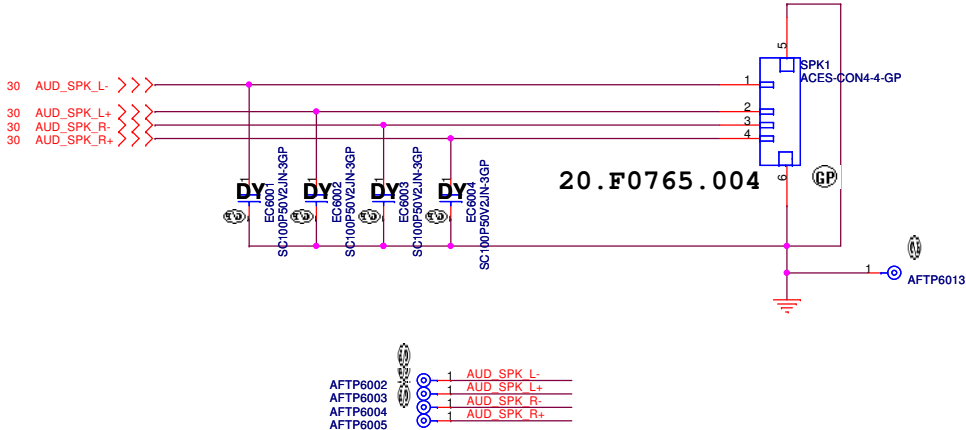


ODD Connector

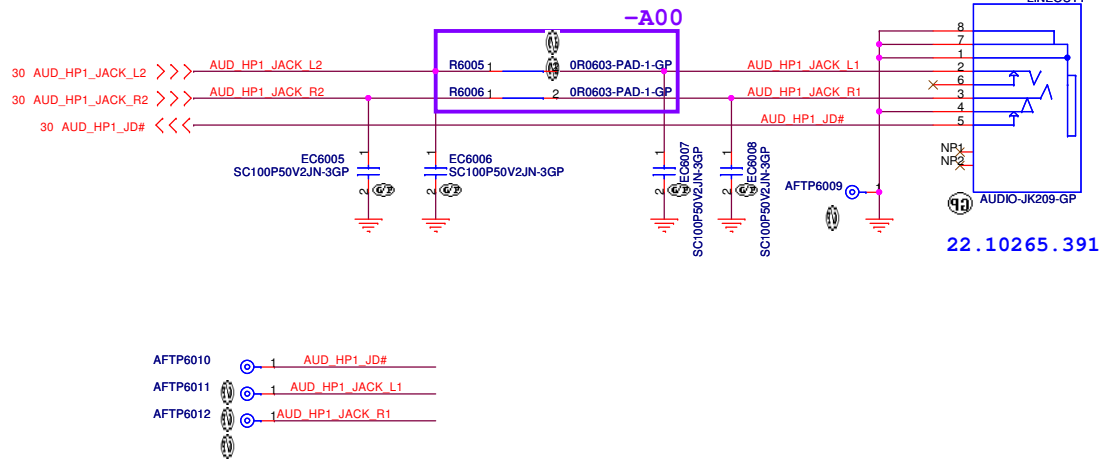


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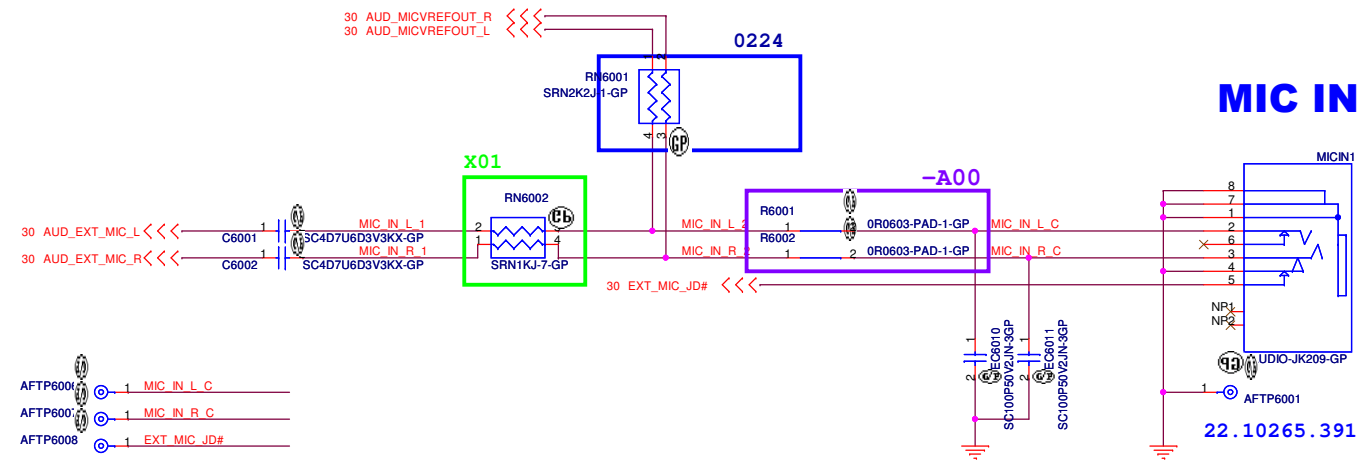
Speaker Connector



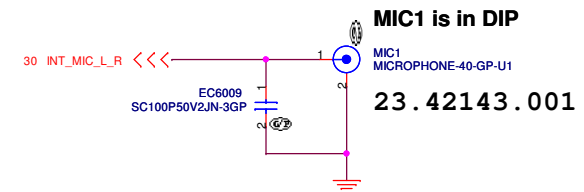
LINE1 OUT



MIC IN



Internal Microphone



SSID = RBATT



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Title

Flash/RTC

Size
A3

Document Number

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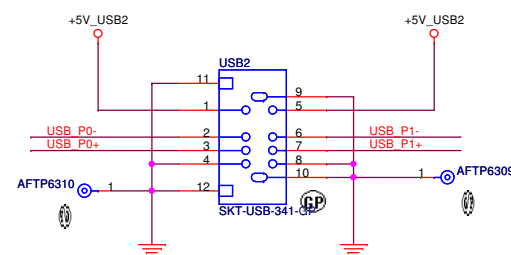
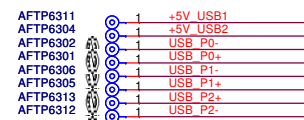
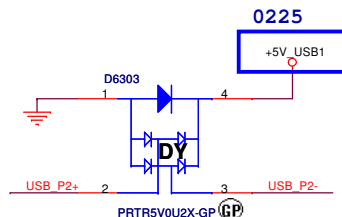
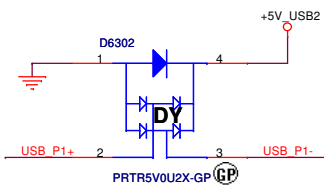
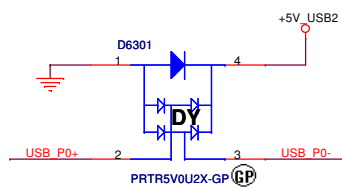
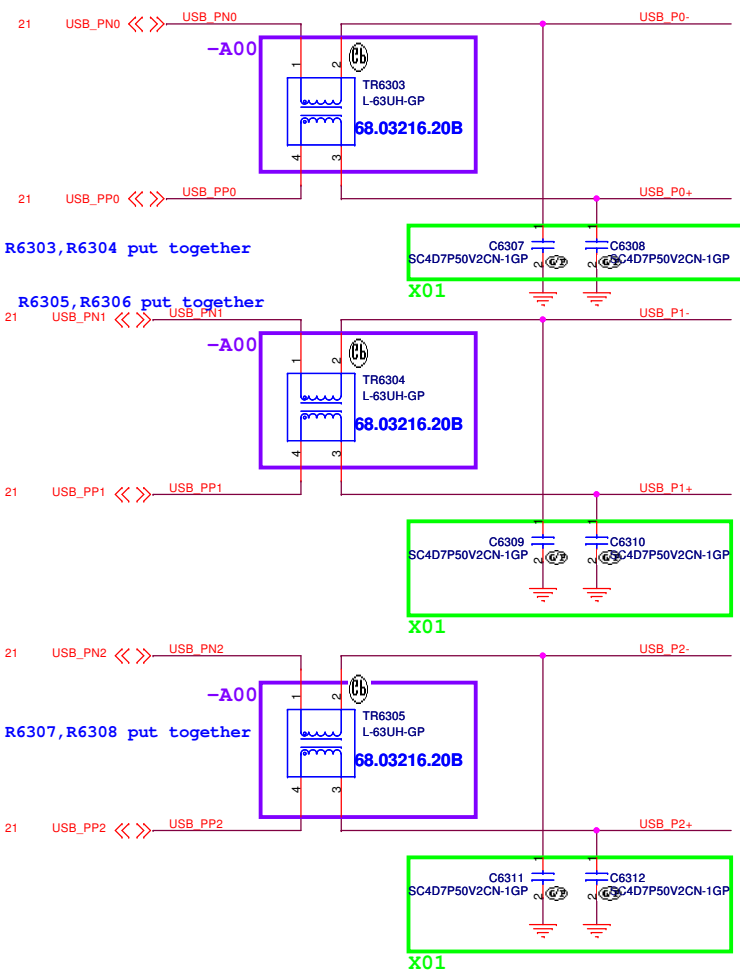
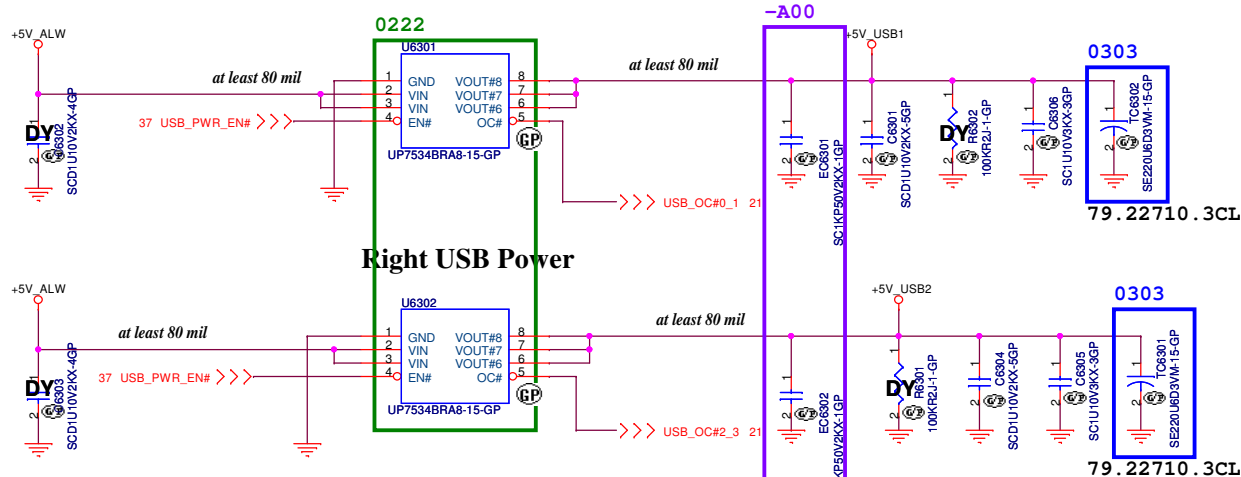
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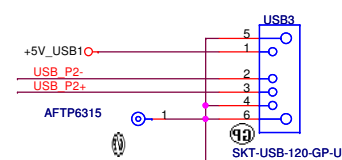
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SSID = USB

USB Power



22.10254.501



22.10218.K71

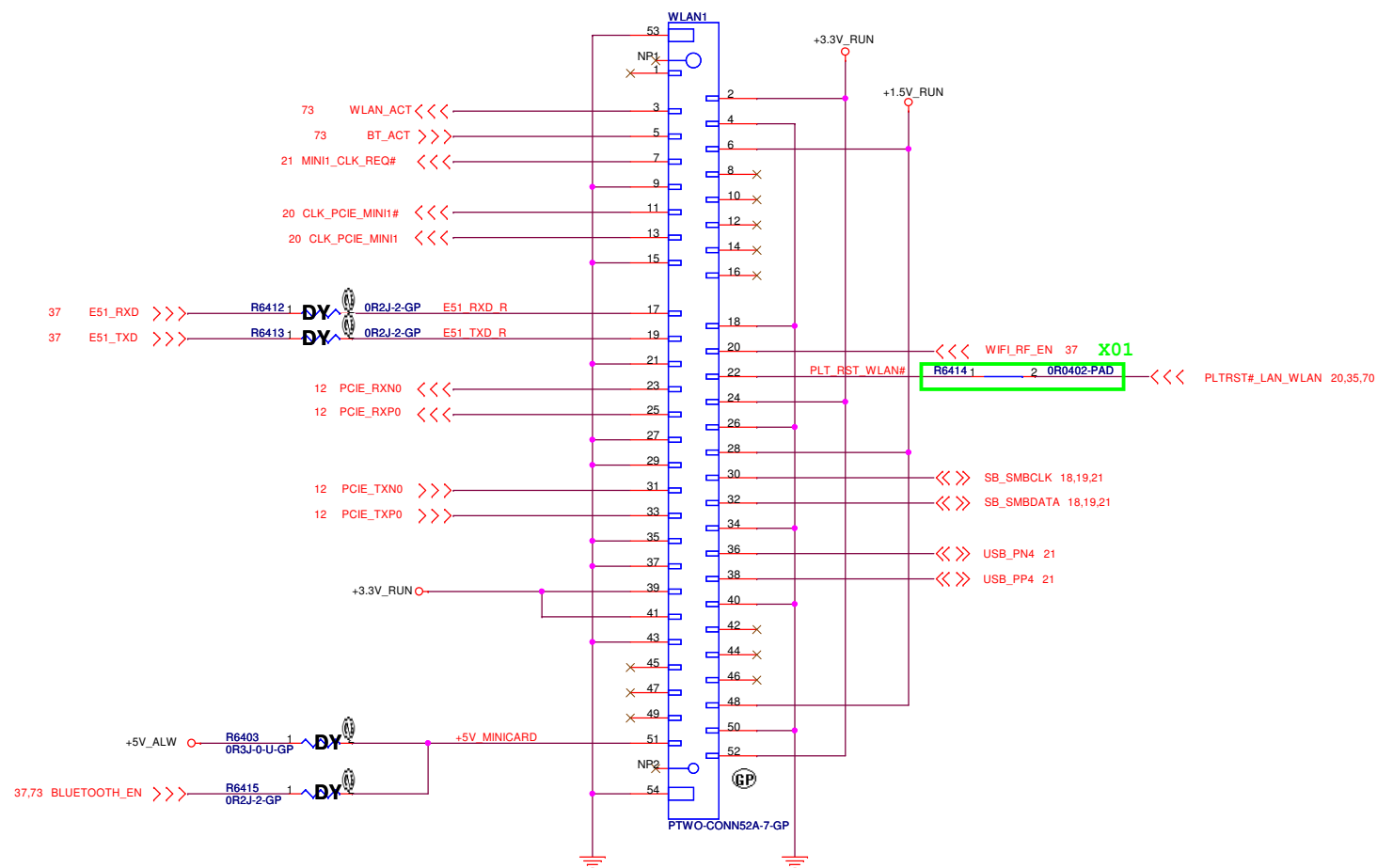
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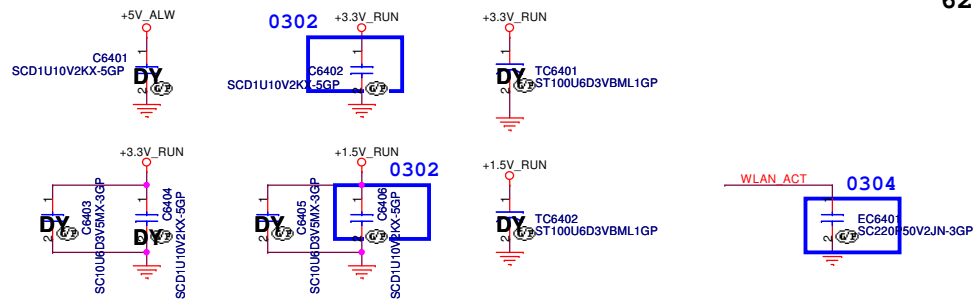
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Title			USB		
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Mini Card Connector(802.11a/b/g)




20.F1516.052
62.10043.771



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Title

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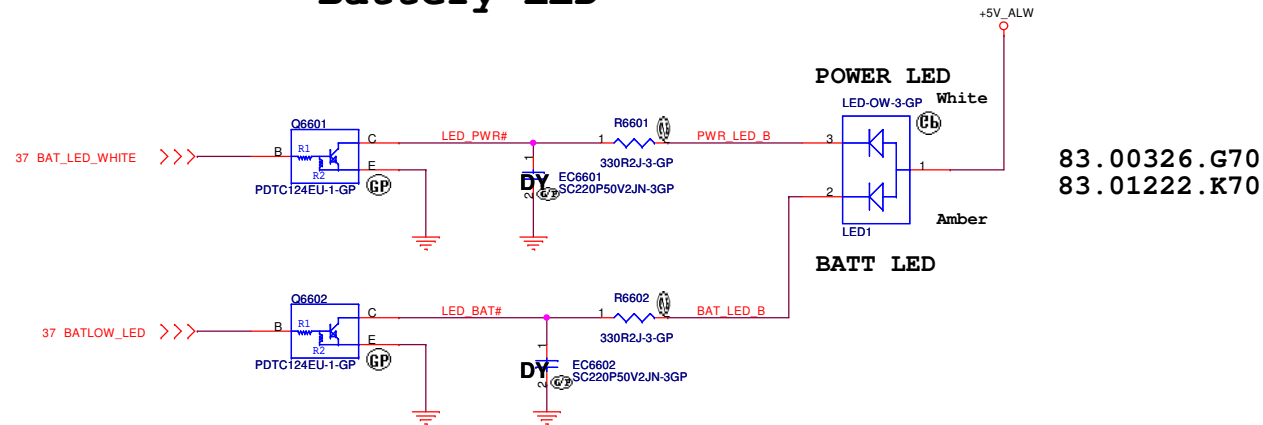
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Document Number
Chelsea DJ2 AMD UMA

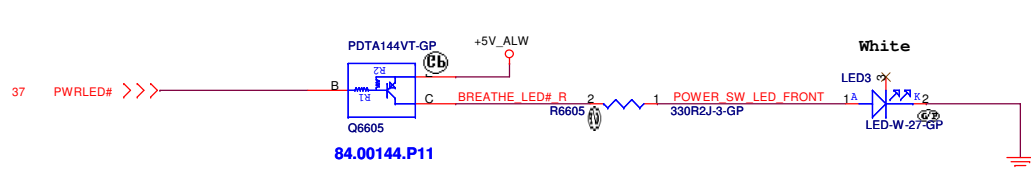
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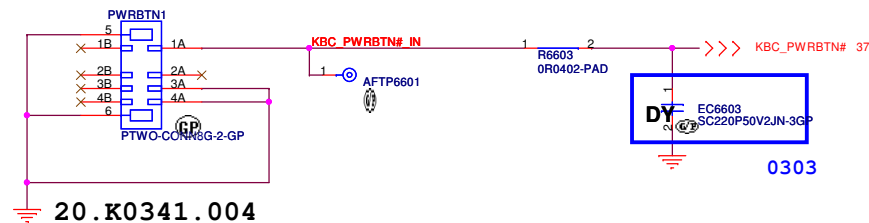
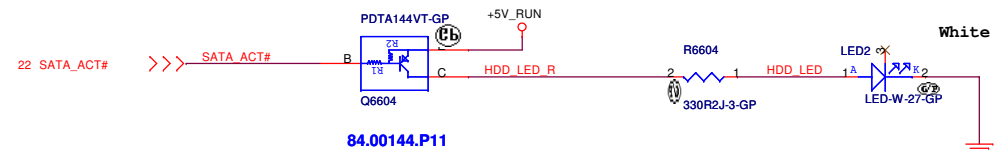
Battery LED



BREATHE PWR LED (Front)



HDD LED




Main DJ1 AMD UMA



Title			LED/PWRBTN	
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Taipei Hsien 221, Taiwan, R.O.C.

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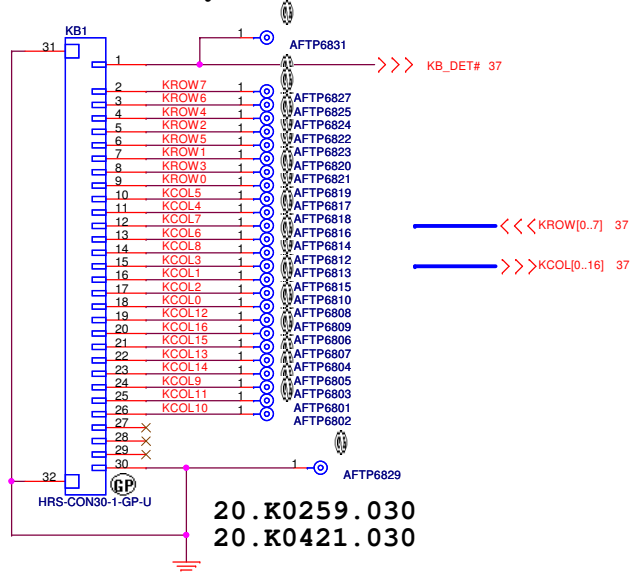
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A3	Chelsea DJ2 AMD UMA	A00

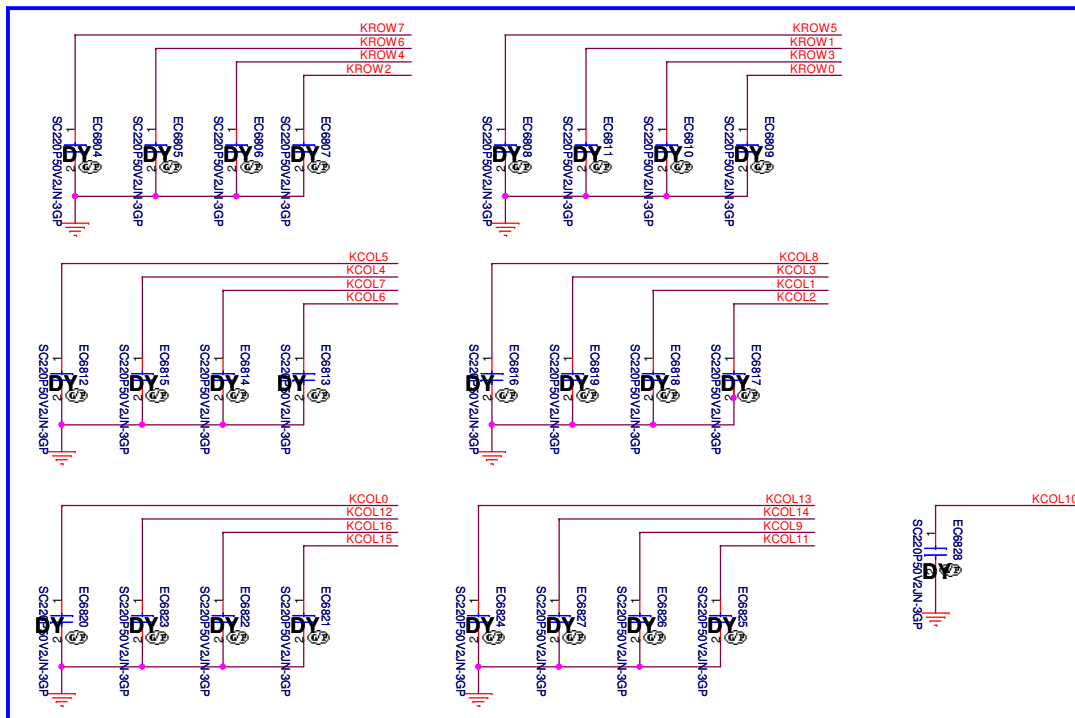
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SSID = KBC

Internal KeyBoard Connector

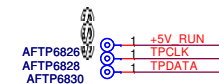
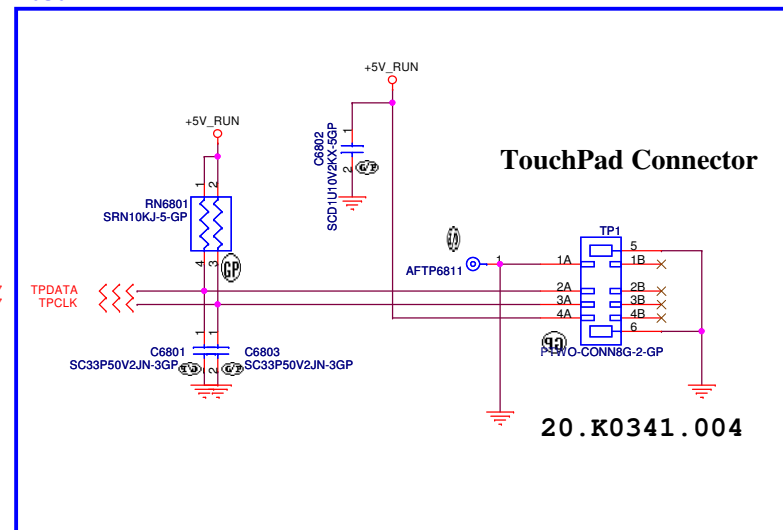


0304

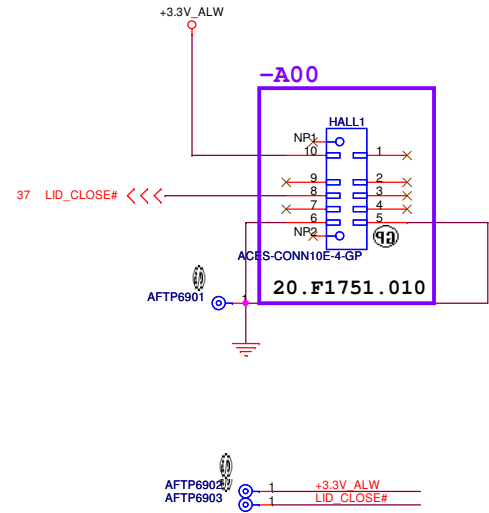


SSID = Touch.Pad

0302



SSID = User. Interface



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Hall Sensor

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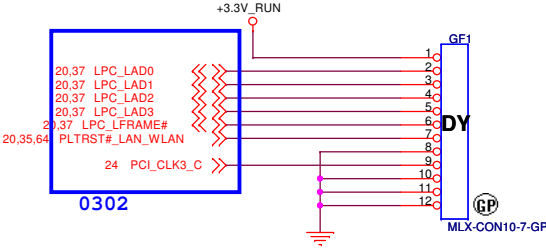
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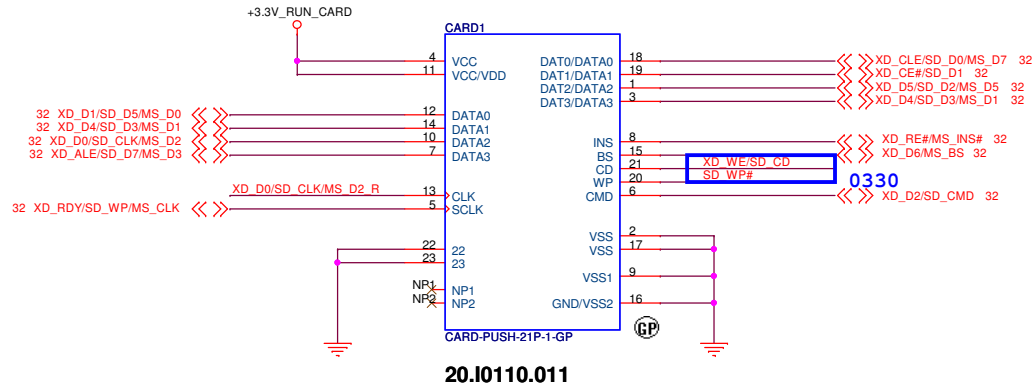
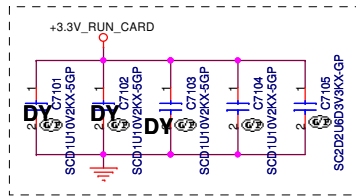
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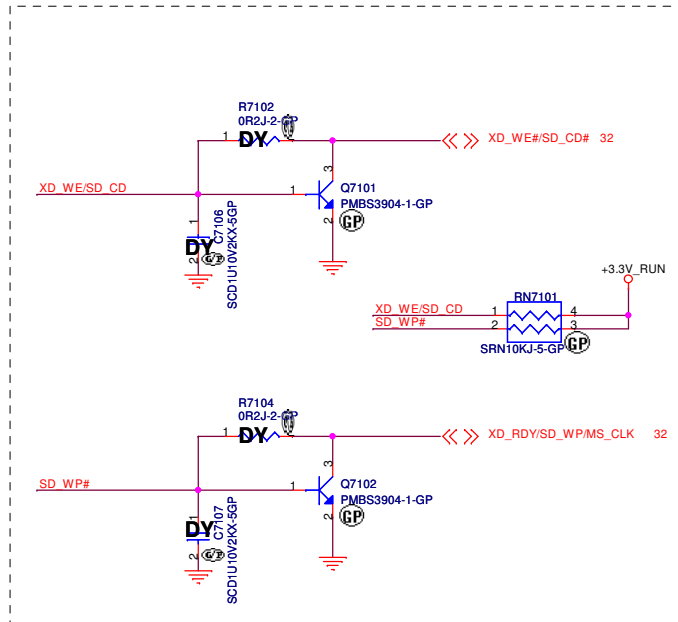


SD/XD/MS Card Reader

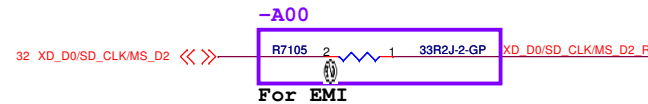
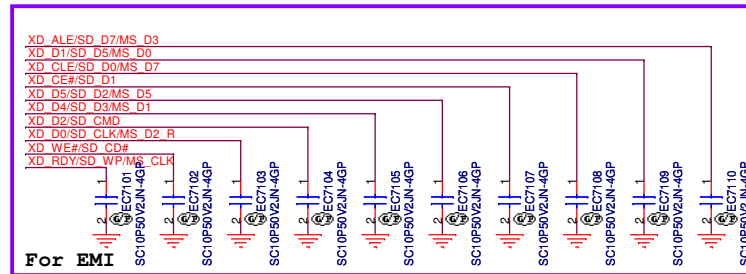
SSID = SDIO



For reverse card connector 0330




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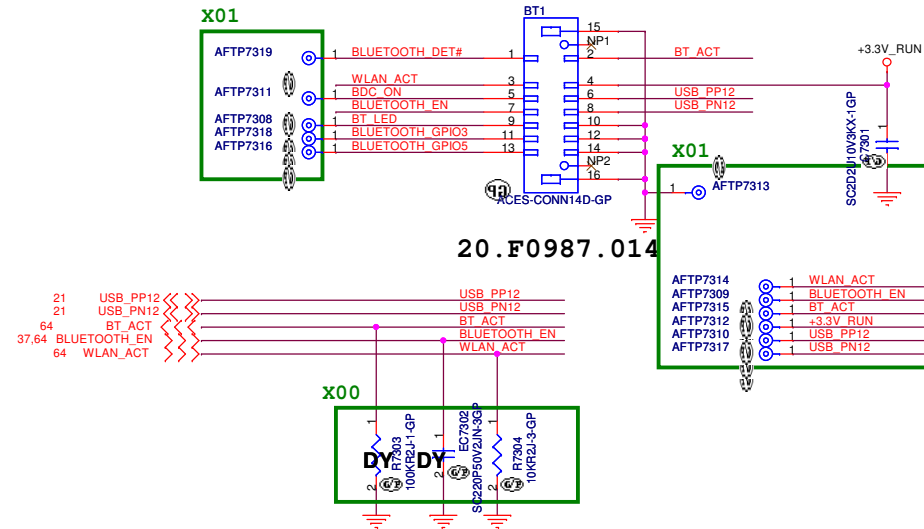
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SSID = User.Interface

Bluetooth Module conn.



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Bluetooth

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IO Board Connector

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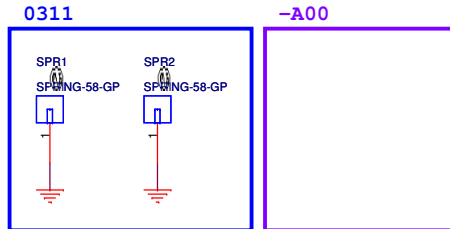
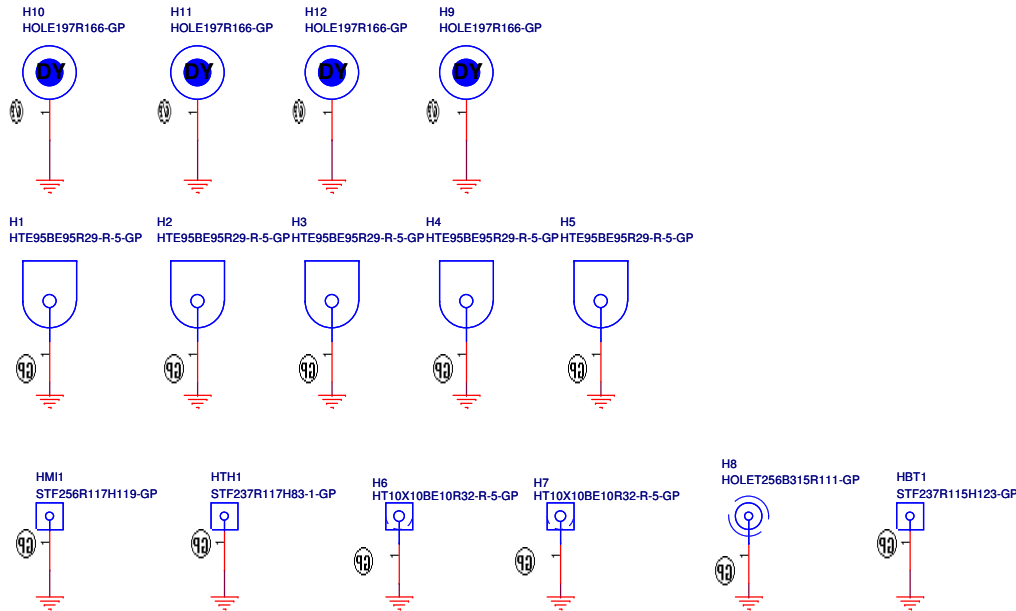
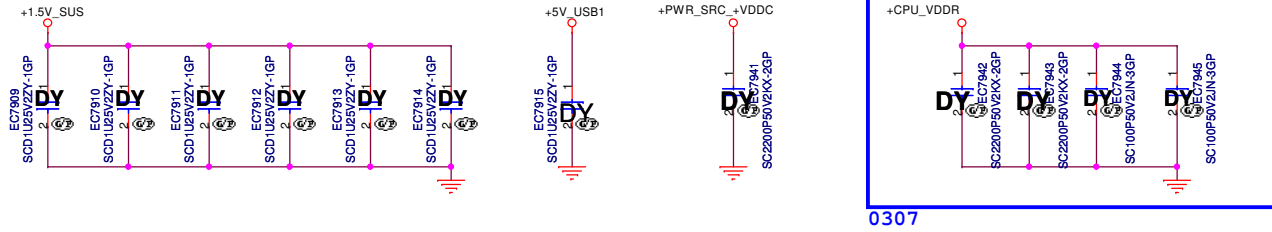
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EMI Request



Main DJ1 AMD UMA

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VGA PCIE(1/4)

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VGA LVDS/TV/CRT(2/4)

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VGA POWER/GND(3/4)

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VGA MEMORY/STRAPS(4/4)

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GPU-VRAM (2/2)

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TPS51117 +VCC GFXCORE

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APL5930 +1.1V RUN

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DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
		1	37	pop R3729 , depop R3733	MB version	EE
		2	37	DY R3712	compare DJ1 and DJ2 (for battery)	EE
		3	71	add R7101~R7104; C7106~C7107; Q7101~Q7102	For reversal cardreader connector	EE
						EE
		5	70	depop GF1	non-pop debug port	EE
		6	42	C4203 from 100pF to 4.7nF	For sequence	EE
		7	61	reserve U6103, U5104, U6105	For LAN Surge	EE
		8	47	PR4720 change to 95.3Kohm(64.95325.6DL) . PR4721 change to 22Kohm(64.22025.6DL) .	For CPU_CORE OCP	EE
		9	20	RN2006 from 0R to 10R	For CLK_LAN slew rate fail	EE
		10	55	C5508~C5510 from 8.2pF to 10pF L5501~L5503 change to 33 ohm bead	For EMI request	EMI
		11	79	add SPR3 and SPR4	For EMI request	EMI
		12	63 21	add C6307~C6312 ; C2106~C2107 4.7pF	Fine tune USB signal	EE
	A00	1	22	add R2131 pull high +3.3V_ALW	no internal pull-high	EE
		2	37	add R3717 pull down	to select DJ2 KBC code	EE
		3	38	Paste R3730, Dumm R3734	MB version	EE
		4	49	PR4905 PWR change from +3.3V_ALW to +3.3V_RUN	PWR saving	EE
		5	39	Dummy D3901 paste R3915	For Fan	EE
		6	30	AMP_MUTE# reconnect	For Audio anti-pop	EE
		7	69	HALL1 change to 20.F1751.010	connector change	ME
		8	54	paste PC4504	PWR team request	PWR
		9	24	Dummy ER2401		EE
		10		Short PAD R1329,R2304,R3023,R3024,R3025,R3026,R3027 R3031,R6001,R6002,R6005,R6006		EE
		11		Short PAD R2303,R3732,R3751,R3757,R3906,R6203,R6205		EE

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